

# TCA9534 Low Voltage 8-Bit I<sup>2</sup>C and SMBUS Low-Power I/O Expander with Interrupt Output and Configuration Registers

## 1 Features

- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)
- Low Standby Current Consumption
- I<sup>2</sup>C to Parallel Port Expander
- Open-Drain Active-Low Interrupt Output
- Operating Power-Supply Voltage Range of 1.65 V to 5.5 V
- 5-V Tolerant I/O Ports
- 400-kHz Fast I<sup>2</sup>C Bus
- Three Hardware Address Pins Allow up to Eight Devices on the I<sup>2</sup>C/SMBus
- Input and Output Configuration Register
- Polarity Inversion Register
- Internal Power-On Reset
- Power-Up With All Channels Configured as Inputs
- No Glitch on Power Up
- Noise Filter on SCL/SDA Inputs
- Latched Outputs With High-Current Drive Maximum Capability for Directly Driving LEDs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

## 2 Applications

- Servers
- Routers (Telecom Switching Equipment)
- Personal Computers
- Personal Electronics (for example: Gaming Consoles)
- Industrial Automation
- Products With GPIO-Limited Processors

## 3 Description

The TCA9534 is a 16-pin device that provides 8 bits of general purpose parallel input and output (I/O) expansion for the two-line bidirectional I<sup>2</sup>C bus (or SMBus) protocol. The device can operate with a power supply voltage ranging from 1.65 V to 5.5 V, which allows for use with a wide range of devices. The device supports both 100-kHz (Standard-mode) and 400-kHz (Fast-mode) clock frequencies. I/O expanders such as the TCA9534 provide a simple solution when additional I/Os are needed for switches, sensors, push-buttons, LEDs, fans, and other similar devices.

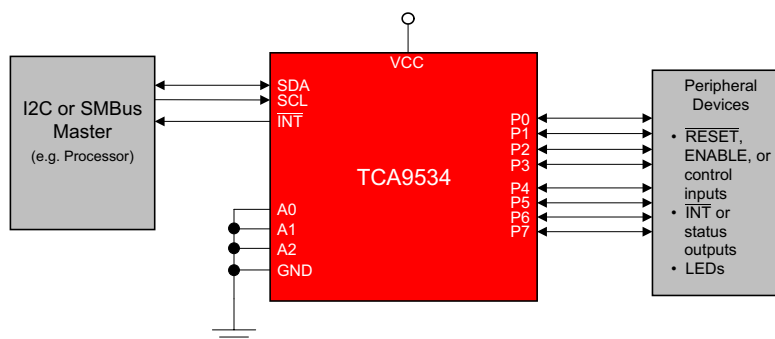
The features of the TCA9534 include an interrupt that is generated on the  $\overline{\text{INT}}$  pin. This allows the master to know when an input port changes state. The A0, A1, and A2 hardware selectable address pins allow up to eight TCA9534 devices on the same I<sup>2</sup>C bus. The device can also be reset to its default state by cycling the power supply and causing a power-on reset.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TCA9534	TSSOP (16)	5.00 mm x 4.40 mm
	SOIC (16)	10.30 mm x 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

### Simplified Schematic



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (February 2017) to Revision D	Page
• Changed V <sub>IH</sub> value From: V <sub>CC</sub> = 1.65 V to 2.7 V To: V <sub>CC</sub> = 1.65 V to 5.5 V in the <i>Recommended Operating Condition</i> .....	5
• Changed V <sub>IL</sub> value From: V <sub>CC</sub> = 1.65 V to 2.7 V To: V <sub>CC</sub> = 1.65 V to 5.5 V in the <i>Recommended Operating Condition</i> .....	5

Changes from Revision B (November 2016) to Revision C	Page
• Added MAX value: 2000 to V <sub>CC_FT</sub> and V <sub>CC_RT</sub> in <i>Recommended Supply Sequencing and Ramp Rates</i> table.....	27
• Changed V <sub>CC_TRR</sub> MIN value from: "2" to: "1" in <i>Recommended Supply Sequencing and Ramp Rates</i> table .....	27

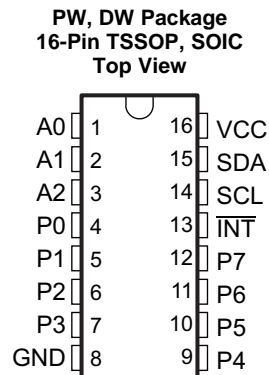
Changes from Revision A (September 2014) to Revision B	Page
• Updated the <i>Description</i> section.....	1
• Added DW package.....	1
• Corrected ESD ratings to reflect ± ratings.....	5
• V <sub>IH</sub> values, improved performance in the <i>Recommended Operating Condition</i> .....	5
• Made changes to I <sub>OL</sub> in the <i>Recommended Operating Condition</i> table .....	5
• Changed V <sub>PORR</sub> limits in the <i>Electrical Characteristics</i> table .....	6
• Changed V <sub>OH</sub> at V <sub>CC</sub> = 1.65 V in the <i>Electrical Characteristics</i> table .....	6
• Updated I <sub>OL</sub> in the <i>Electrical Characteristics</i> table.....	6
• Changed I <sub>CC</sub> in the <i>Electrical Characteristics</i> table .....	7
• Deleted ΔI <sub>CC</sub> parameter from the <i>Electrical Characteristics</i> table .....	7
• Increased the pin capacitance maximum, decreased typical in the <i>Electrical Characteristics</i> table.....	7
• Updated graphs in <i>Typical Characteristics</i> section .....	9
• Updated <i>Interrupt Output (INT)</i> section .....	17
• Added the <i>Calculating Junction Temperature and Power Dissipation</i> section.....	25

- Added  $V_{CC\_MV}$  to [Table 8](#) ..... 27
  - Updated [Figure 39](#) ..... 27
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<b>Changes from Original (September 2014) to Revision A</b>	<b>Page</b>
• Initial release of full version. ....	<b>1</b>

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## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	A0	I	Address input. Connect directly to V <sub>CC</sub> or ground
2	A1	I	Address input. Connect directly to V <sub>CC</sub> or ground
3	A2	I	Address input. Connect directly to V <sub>CC</sub> or ground
4	P0	I/O	P-port input-output. Push-pull design structure. At power on, P0 is configured as an input
5	P1	I/O	P-port input-output. Push-pull design structure. At power on, P1 is configured as an input
6	P2	I/O	P-port input-output. Push-pull design structure. At power on, P2 is configured as an input
7	P3	I/O	P-port input-output. Push-pull design structure. At power on, P3 is configured as an input
8	GND	—	Ground
9	P4	I/O	P-port input-output. Push-pull design structure. At power on, P4 is configured as an input
10	P5	I/O	P-port input-output. Push-pull design structure. At power on, P5 is configured as an input
11	P6	I/O	P-port input-output. Push-pull design structure. At power on, P6 is configured as an input
12	P7	I/O	P-port input-output. Push-pull design structure. At power on, P7 is configured as an input
13	INT	O	Interrupt output. Connect to V <sub>CC</sub> through a pullup resistor
14	SCL	I/O	Serial clock bus. Connect to V <sub>CC</sub> through a pullup resistor
15	SDA	I/O	Serial data bus. Connect to V <sub>CC</sub> through a pullup resistor
16	VCC	—	Supply voltage

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	-0.5	6	V
V <sub>I</sub>	Input voltage <sup>(2)</sup>	-0.5	6	V
V <sub>O</sub>	Output voltage <sup>(2)</sup>	-0.5	6	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-20 mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-20 mA
I <sub>IOK</sub>	Input-output clamp current	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>		±20 mA
I <sub>OL</sub>	Continuous output low current through a single P-port	V <sub>O</sub> = 0 to V <sub>CC</sub>		50 mA
I <sub>OH</sub>	Continuous output high current through a single P-port	V <sub>O</sub> = 0 to V <sub>CC</sub>		-50 mA
I <sub>CC</sub>	Continuous current through GND by all P-ports, $\overline{\text{INT}}$ , and SDA			250 mA
	Continuous current through V <sub>CC</sub> by all P-ports			-160 mA
T <sub>J(MAX)</sub>	Maximum junction temperature			100 °C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	1.65	5.5	V
V <sub>IH</sub>	High-level input voltage	SCL, SDA	V <sub>CC</sub> = 1.65 V to 5.5 V	0.7 × V <sub>CC</sub> V <sub>CC</sub> <sup>(1)</sup>
		A0, A1, A2, P7–P0	V <sub>CC</sub> = 1.65 V to 5.5 V	0.7 × V <sub>CC</sub> 5.5
V <sub>IL</sub>	Low-level input voltage	SCL, SDA	V <sub>CC</sub> = 1.65 V to 5.5 V	-0.5 0.3 × V <sub>CC</sub>
		A0, A1, A2, P7–P0	V <sub>CC</sub> = 1.65 V to 5.5 V	-0.5 0.3 × V <sub>CC</sub>
			V <sub>CC</sub> = 3 V to 5.5 V	-0.5 0.2 × V <sub>CC</sub>
I <sub>OH</sub>	High-level output current	Any P-port, P7–P0		-10 mA
I <sub>OL</sub> <sup>(2)</sup>	Low-level output current	P00–P07, P10–P17	T <sub>J</sub> ≤ 65°C	25
			T <sub>J</sub> ≤ 85°C	18
			T <sub>J</sub> ≤ 105°C	9
		$\overline{\text{INT}}$ , SDA	T <sub>J</sub> ≤ 85°C	6
			T <sub>J</sub> ≤ 105°C	3
I <sub>CC</sub>	Continuous current through GND	All P-ports P7-P0, $\overline{\text{INT}}$ , and SDA		200 mA
	Continuous current through V <sub>CC</sub>	All P-ports P7-P0		-80 mA
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

- (1) The SCL and SDA pins shall not be at a higher potential than the supply voltage V<sub>CC</sub> in the application, or an increase in leakage current, I<sub>I</sub>, results.
- (2) The values shown apply to specific junction temperatures. See the [Calculating Junction Temperature and Power Dissipation](#) section on how to calculate the junction temperature.

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TCA9534		UNIT
		PW (TSSOP)	DW (SOIC)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	122	92.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.4	53.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.1	56.9	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	10.8	26.4	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	66.5	56.4	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$V_{CC}$	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{IK}$	Input diode clamp voltage	$I_I = -18$ mA	1.65 V to 5.5 V	-1.2			V
$V_{PORR}$	Power-on reset voltage, $V_{CC}$ rising	$V_I = V_{CC}$ or GND, $I_O = 0$			1.2	1.5	V
$V_{PORF}$	Power-on reset voltage, $V_{CC}$ falling	$V_I = V_{CC}$ or GND, $I_O = 0$		0.75	1		V
$V_{OH}$	P-port high-level output voltage <sup>(2)</sup>	$I_{OH} = -8$ mA	1.65 V	1.2			V
			2.3 V	1.8			
			3 V	2.6			
			4.5 V	4.1			
		$I_{OH} = -10$ mA	1.65 V	1			
			2.3 V	1.7			
			3 V	2.5			
			4.5 V	4			
$I_{OL}$	SDA <sup>(3)</sup>	$V_{OL} = 0.4$ V	1.65 V to 5.5 V	3			mA
	P port <sup>(4)</sup>	$V_{OL} = 0.5$ V	1.65 V to 5.5 V	8			
		$V_{OL} = 0.7$ V	1.65 V to 5.5 V	10			
	$\overline{INT}$ <sup>(5)</sup>	$V_{OL} = 0.4$ V	1.65 V to 5.5 V	3			
$I_I$	SCL, SDA	$V_I = V_{CC}$ or GND	1.65 V to 5.5 V			$\pm 1$	$\mu$ A
	A0, A1, A2					$\pm 1$	
$I_{IH}$	P port	$V_I = V_{CC}$	1.65 V to 5.5 V			1	$\mu$ A
$I_{IL}$	P port	$V_I = GND$	1.65 V to 5.5 V			-1	$\mu$ A

(1) All typical values are at nominal supply voltage (1.8-, 2.5-, 3.3-, or 5-V  $V_{CC}$ ) and  $T_A = 25^\circ\text{C}$ .

(2) Each P-port I/O configured as a high output must be externally limited to a maximum of 10 mA, and the total current sourced by all I/Os (P-ports P7-P0) through  $V_{CC}$  must be limited to a maximum current of 80 mA.

(3) The SDA pin must be externally limited to a maximum of 12 mA, and the total current sunk by all I/Os (P-ports P7-P0,  $\overline{INT}$ , and SDA) through GND must be limited to a maximum current of 200 mA.

(4) Each P-port I/O configured as a low output must be externally limited to a maximum of 25 mA, and the total current sunk by all I/Os (P-ports P7-P0,  $\overline{INT}$ , and SDA) through GND must be limited to a maximum current of 200 mA.

(5) The  $\overline{INT}$  pin must be externally limited to a maximum of 7 mA, and the total current sunk by all I/Os (P-ports P7-P0,  $\overline{INT}$ , and SDA) through GND must be limited to a maximum current of 200 mA.

## Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT		
I <sub>CC</sub>	Operating mode	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0, I/O = inputs, f <sub>SCL</sub> = 400 kHz, no load		5.5 V		22	40	μA		
				3.6 V		11	30			
				2.7 V		8	19			
				1.95 V		5	11			
	Standby mode	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0, I/O = inputs, f <sub>SCL</sub> = 0 kHz, no load		V <sub>I</sub> = V <sub>CC</sub>		5.5 V			1.5	3.9
				V <sub>I</sub> = V <sub>CC</sub>		3.6 V			0.9	2.2
				V <sub>I</sub> = V <sub>CC</sub>		2.7 V			0.6	1.8
				V <sub>I</sub> = V <sub>CC</sub>		1.95 V			0.4	1.5
				V <sub>I</sub> = GND		5.5 V			1.5	8.7
				V <sub>I</sub> = GND		3.6 V			0.9	4
V <sub>I</sub> = GND		2.7 V		0.6	3					
V <sub>I</sub> = GND		1.95 V		0.4	2.2					
C <sub>i</sub>	SCL	V <sub>I</sub> = V <sub>CC</sub> or GND		1.65 V to 5.5 V		3	8	pF		
C <sub>io</sub>	SDA	V <sub>IO</sub> = V <sub>CC</sub> or GND		1.65 V to 5.5 V		3	9.5	pF		
	P port					3.7	9.5			

## 6.6 I<sup>2</sup>C Interface Timing Requirements

over operating free-air temperature range (unless otherwise noted) (see [Figure 19](#))

				MIN	MAX	UNIT
<b>STANDARD MODE</b>						
f <sub>scl</sub>	I <sup>2</sup> C clock frequency			0	100	kHz
t <sub>sch</sub>	I <sup>2</sup> C clock high time			4		μs
t <sub>scl</sub>	I <sup>2</sup> C clock low time			4.7		μs
t <sub>sp</sub>	I <sup>2</sup> C spike time				50	ns
t <sub>sds</sub>	I <sup>2</sup> C serial-data setup time			250		ns
t <sub>sdh</sub>	I <sup>2</sup> C serial-data hold time			0		ns
t <sub>icr</sub>	I <sup>2</sup> C input rise time				1000	ns
t <sub>icf</sub>	I <sup>2</sup> C input fall time				300	ns
t <sub>ocf</sub>	I <sup>2</sup> C output fall time	10-pF to 400-pF bus			300	ns
t <sub>buf</sub>	I <sup>2</sup> C bus free time between Stop and Start			4.7		μs
t <sub>sts</sub>	I <sup>2</sup> C Start or repeated Start condition setup			4.7		μs
t <sub>sth</sub>	I <sup>2</sup> C Start or repeated Start condition hold			4		μs
t <sub>sps</sub>	I <sup>2</sup> C Stop condition setup			4		μs
t <sub>vd(data)</sub>	Valid data time	SCL low to SDA output valid			3.45	μs
t <sub>vd(ack)</sub>	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low			3.45	μs
C <sub>b</sub>	I <sup>2</sup> C bus capacitive load				400	pF
<b>FAST MODE</b>						
f <sub>scl</sub>	I <sup>2</sup> C clock frequency			0	400	kHz
t <sub>sch</sub>	I <sup>2</sup> C clock high time			0.6		μs
t <sub>scl</sub>	I <sup>2</sup> C clock low time			1.3		μs
t <sub>sp</sub>	I <sup>2</sup> C spike time				50	ns
t <sub>sds</sub>	I <sup>2</sup> C serial-data setup time			100		ns
t <sub>sdh</sub>	I <sup>2</sup> C serial-data hold time			0		ns
t <sub>icr</sub>	I <sup>2</sup> C input rise time			20	300	ns
t <sub>icf</sub>	I <sup>2</sup> C input fall time			20 × (V <sub>DD</sub> / 5.5 V)		ns
t <sub>ocf</sub>	I <sup>2</sup> C output fall time	10-pF to 400-pF bus		20 × (V <sub>DD</sub> / 5.5 V)		ns

## I<sup>2</sup>C Interface Timing Requirements (continued)

 over operating free-air temperature range (unless otherwise noted) (see [Figure 19](#))

		MIN	MAX	UNIT	
$t_{buf}$	I <sup>2</sup> C bus free time between Stop and Start	1.3		μs	
$t_{sts}$	I <sup>2</sup> C Start or repeated Start condition setup	0.6		μs	
$t_{sth}$	I <sup>2</sup> C Start or repeated Start condition hold	0.6		μs	
$t_{sps}$	I <sup>2</sup> C Stop condition setup	0.6		μs	
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		0.9	μs
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		0.9	μs
$C_b$	I <sup>2</sup> C bus capacitive load		400	pF	

## 6.7 Switching Characteristics

 over operating free-air temperature range (unless otherwise noted) (see [Figure 20](#) and [Figure 21](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$t_{iv}$	Interrupt valid time	P port		4	μs
$t_{ir}$	Interrupt reset delay time	SCL		4	μs
$t_{pv}$	Output data valid	SCL		350	ns
$t_{ps}$	Input data setup time	P port	100		ns
$t_{ph}$	Input data hold time	P port	1		μs



## 6.8 Typical Characteristics

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

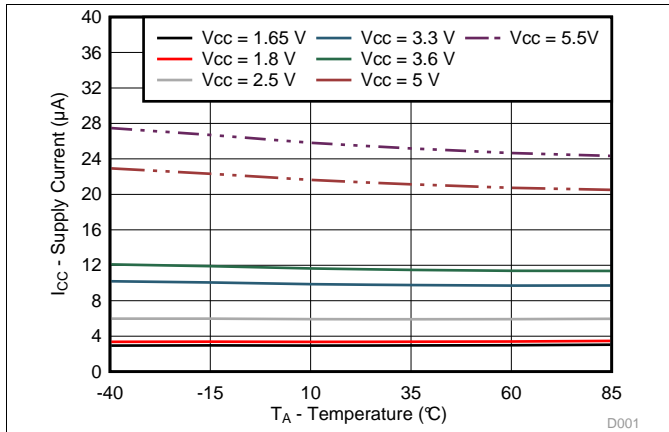


Figure 1. Supply Current vs Temperature for Different Supply Voltage ( $V_{CC}$ )

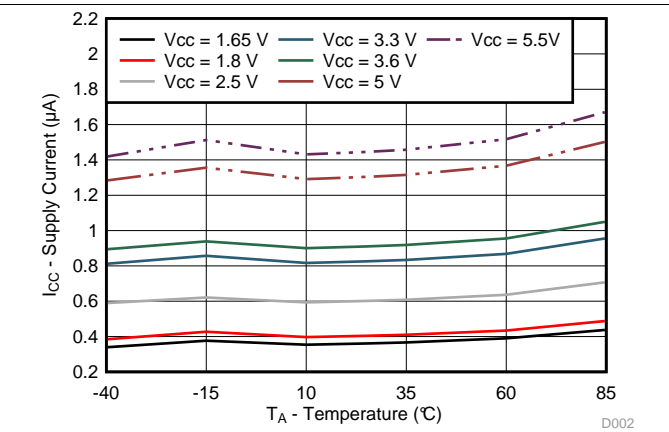


Figure 2. Standby Supply Current vs Temperature for Different Supply Voltage ( $V_{CC}$ )

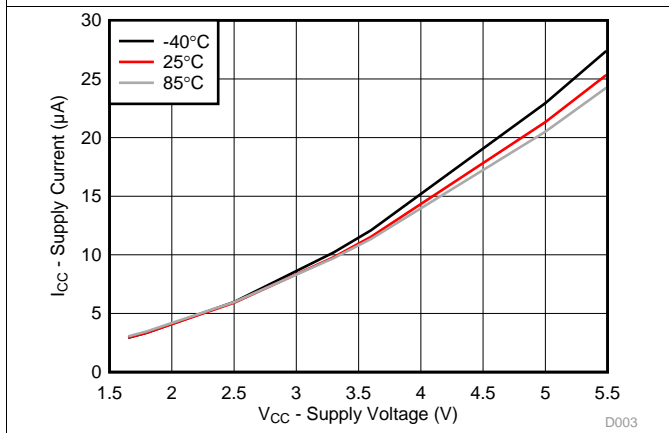


Figure 3. Supply Current vs Supply Voltage for Different Temperature ( $T_A$ )

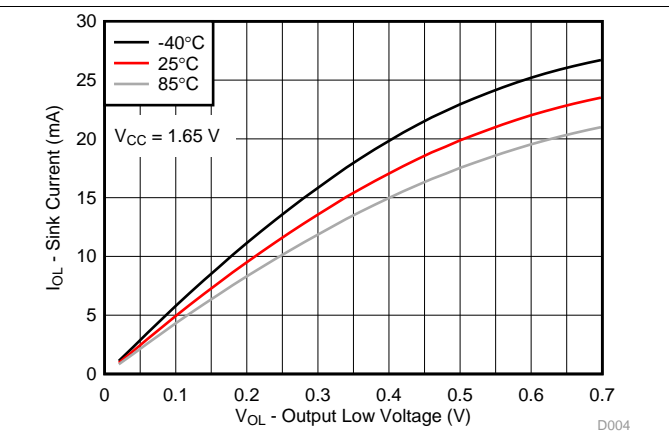


Figure 4. I/O Sink Current vs Output Low Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 1.65\text{ V}$

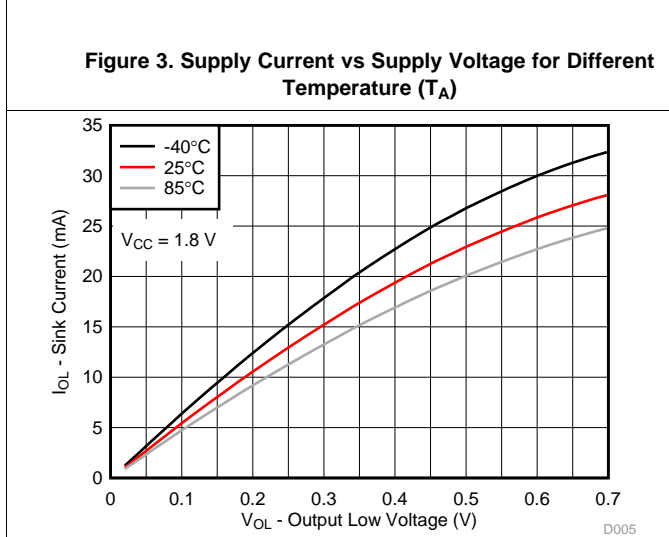


Figure 5. I/O Sink Current vs Output Low Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 1.8\text{ V}$

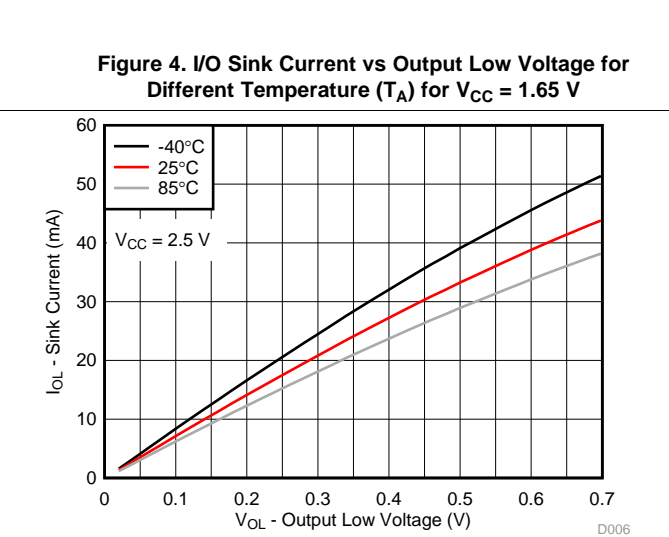


Figure 6. I/O Sink Current vs Output Low Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 2.5\text{ V}$

### Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

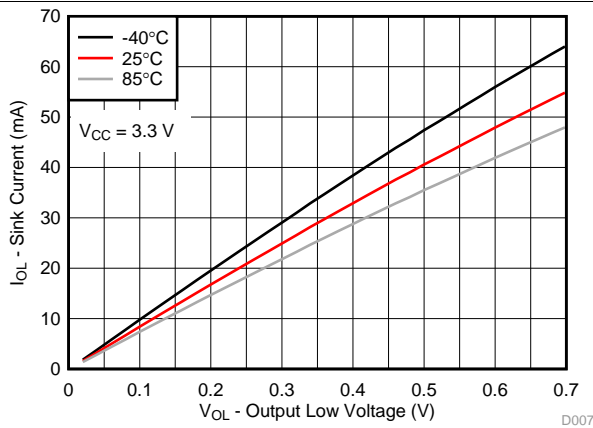


Figure 7. I/O Sink Current vs Output Low Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 3.3\text{ V}$

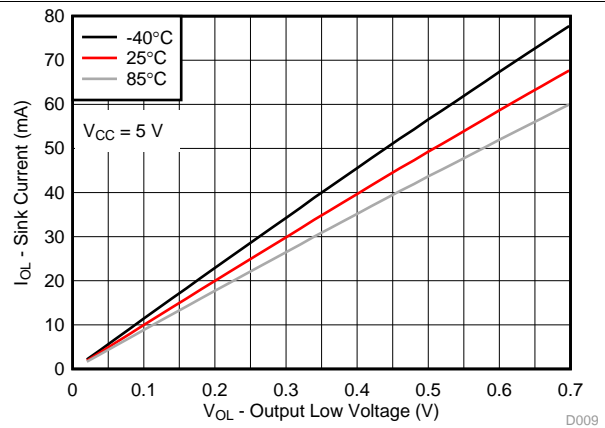


Figure 8. I/O Sink Current vs Output Low Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 5\text{ V}$

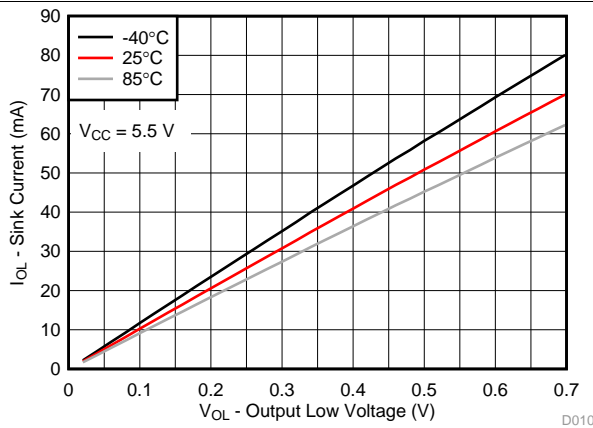


Figure 9. I/O Sink Current vs Output Low Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 5.5\text{ V}$

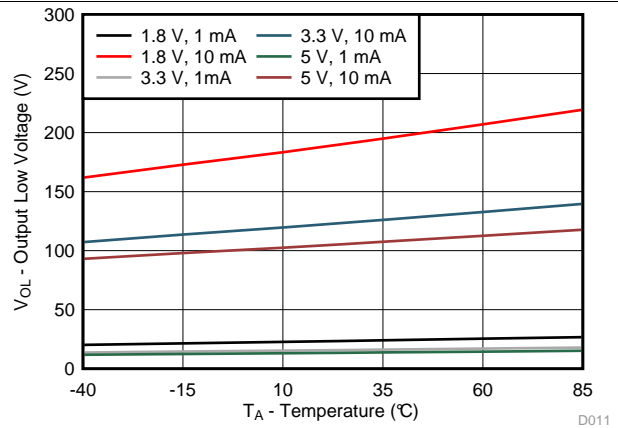


Figure 10. I/O Low Voltage vs Temperature for Different  $V_{CC}$  and  $I_{OL}$

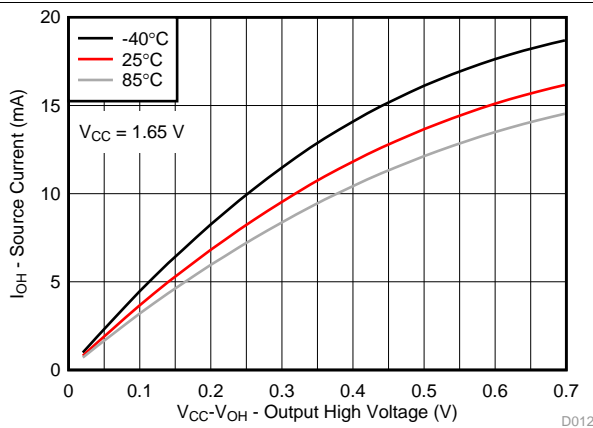


Figure 11. I/O Source Current vs Output High Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 1.65\text{ V}$

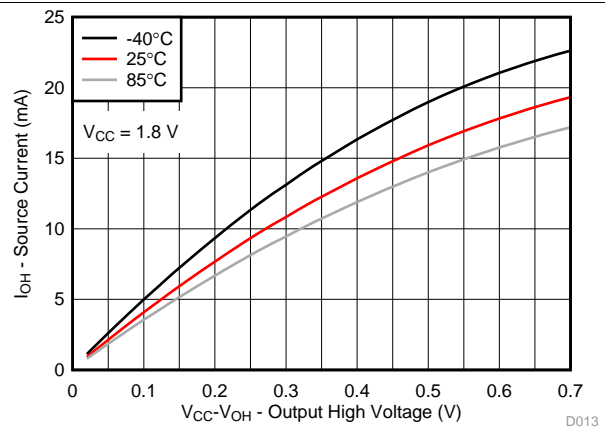


Figure 12. I/O Source Current vs Output High Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 1.8\text{ V}$

Typical Characteristics (continued)

T<sub>A</sub> = 25°C (unless otherwise noted)

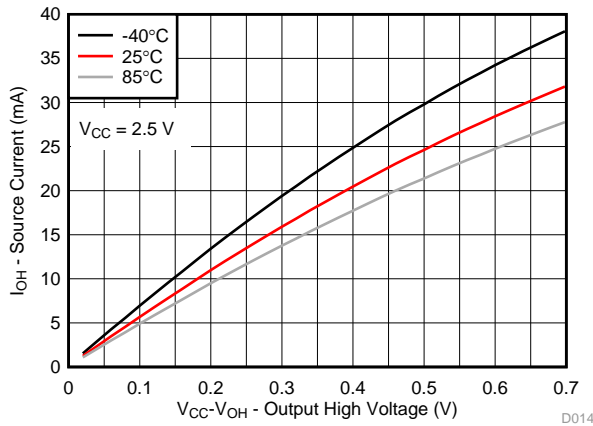


Figure 13. I/O Source Current vs Output High Voltage for Different Temperature (T<sub>A</sub>) for V<sub>CC</sub> = 2.5 V

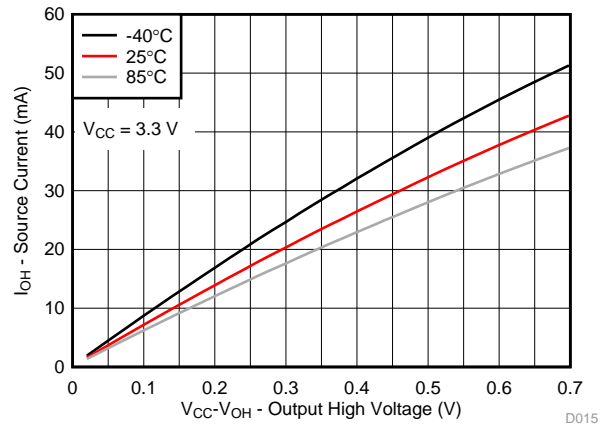


Figure 14. I/O Source Current vs Output High Voltage for Different Temperature (T<sub>A</sub>) for V<sub>CC</sub> = 3.3 V

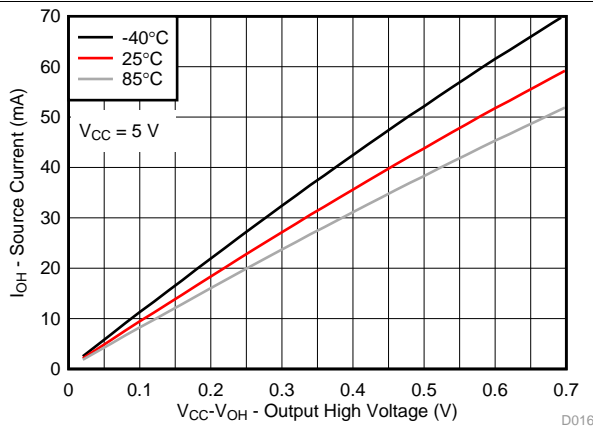


Figure 15. I/O Source Current vs Output High Voltage for Different Temperature (T<sub>A</sub>) for V<sub>CC</sub> = 5 V

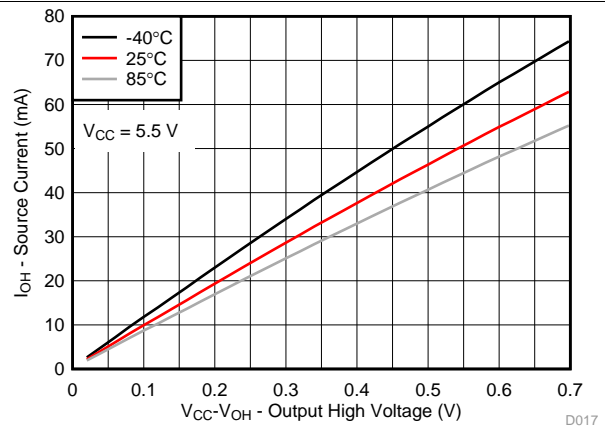


Figure 16. I/O Source Current vs Output High Voltage for Different Temperature (T<sub>A</sub>) for V<sub>CC</sub> = 5.5 V

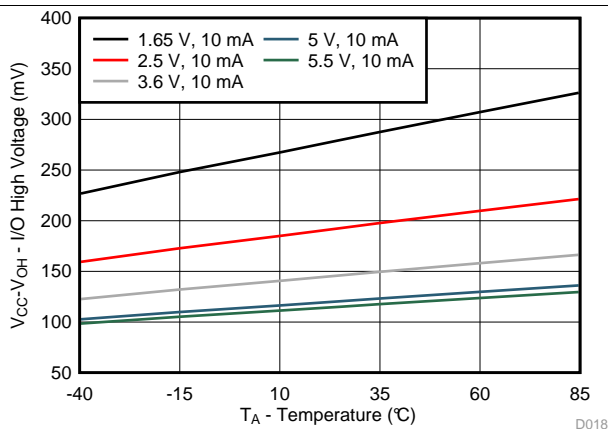


Figure 17. V<sub>CC</sub> - V<sub>OH</sub> Voltage vs Temperature for Different V<sub>CC</sub>

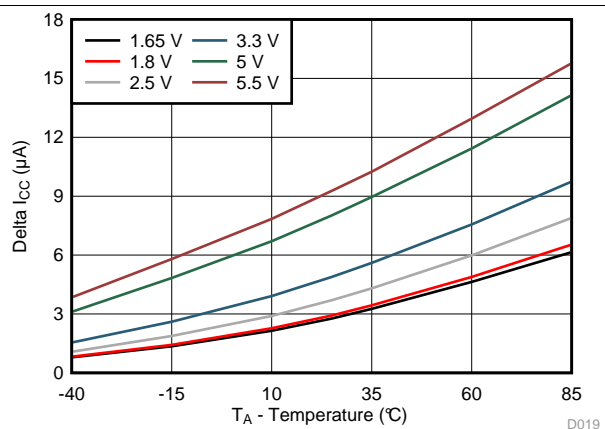
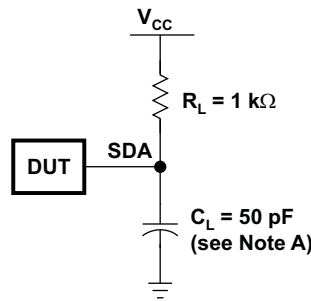
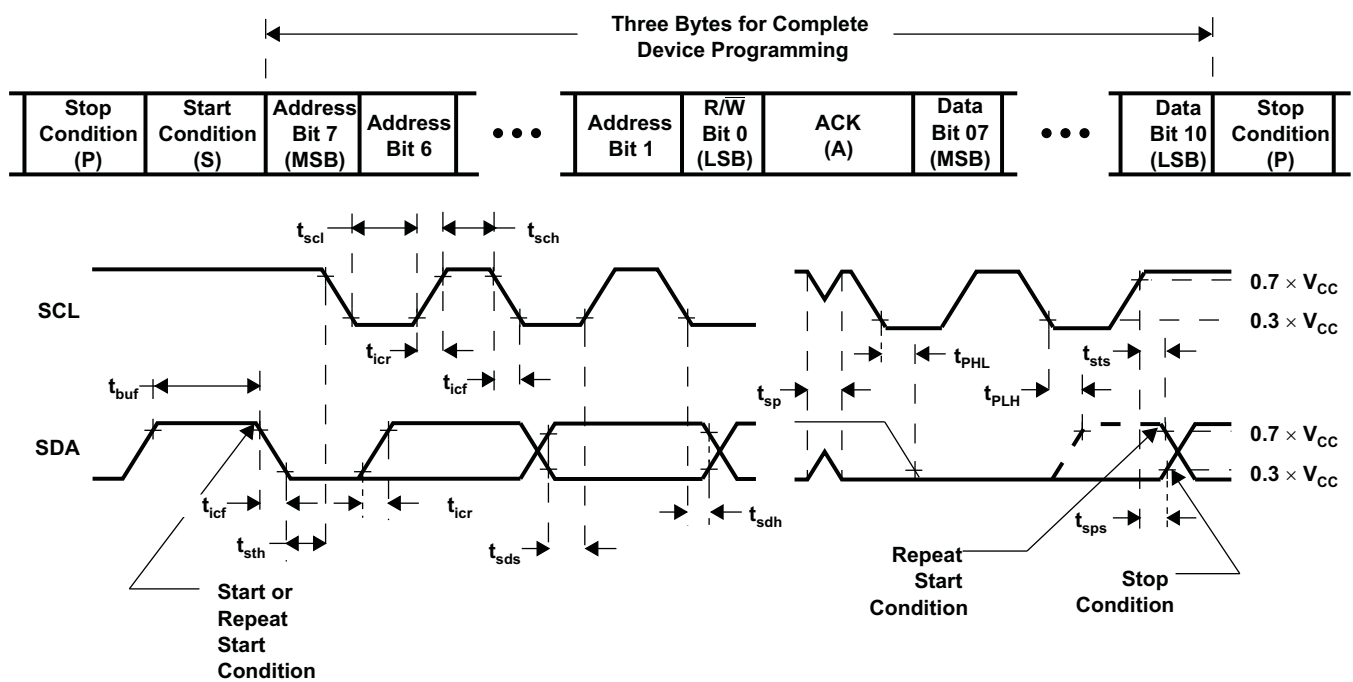


Figure 18. Δ I<sub>CC</sub> vs Temperature for Different V<sub>CC</sub> (V<sub>I</sub> = V<sub>CC</sub> - 0.6 V)

## 7 Parameter Measurement Information



SDA LOAD CONFIGURATION



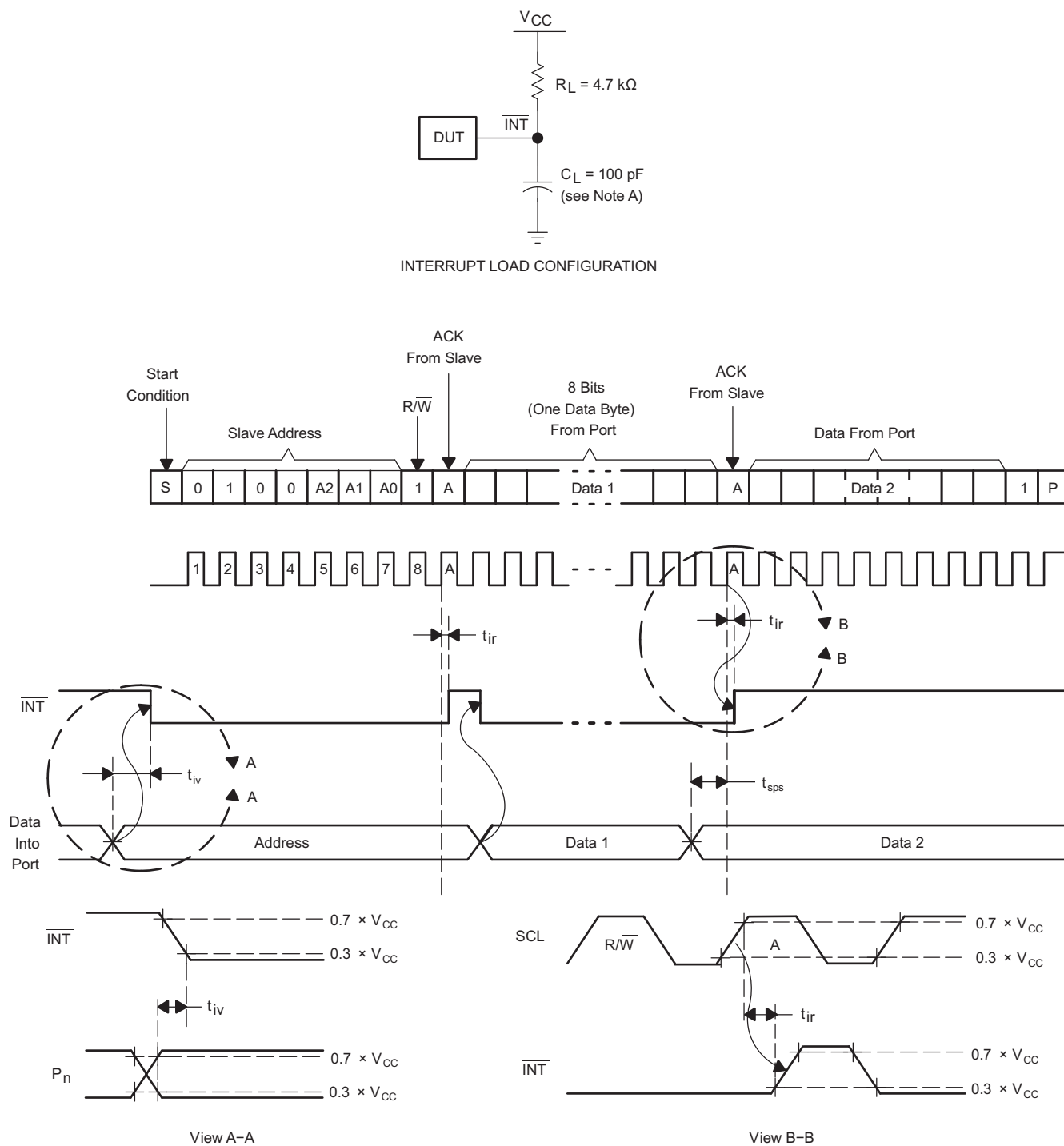
VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I <sup>2</sup> C address
2, 3	P-port data

- A.  $C_L$  includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- C. All parameters and waveforms are not applicable to all devices.

Figure 19. I<sup>2</sup>C Interface Load Circuit and Voltage Waveforms

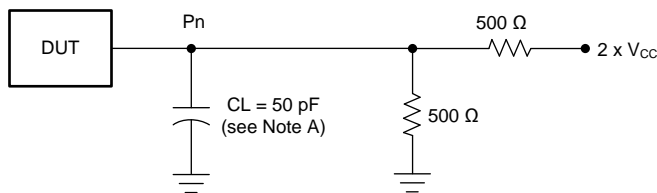
Parameter Measurement Information (continued)



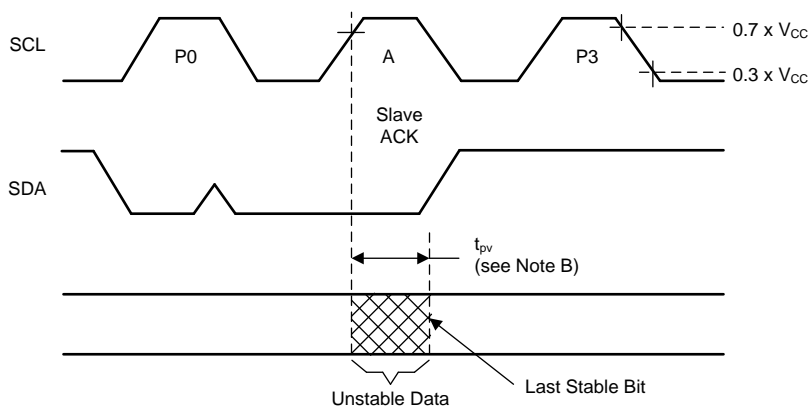
- A.  $C_L$  includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- C. All parameters and waveforms are not applicable to all devices.

Figure 20. Interrupt Load Circuit and Voltage Waveforms

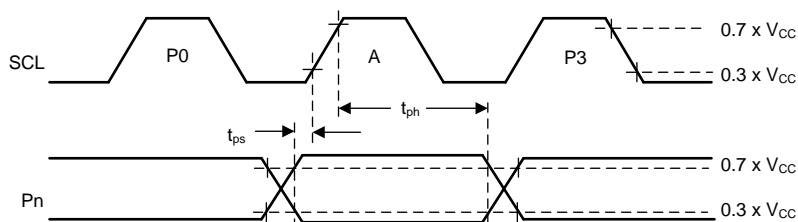
**Parameter Measurement Information (continued)**



P-PORT LOAD CONFIGURATION



WRITE MODE ( $R/\bar{W} = 0$ )



READ MODE ( $R/\bar{W} = 1$ )

- A.  $C_L$  includes probe and jig capacitance.
- B.  $t_{pv}$  is measured from  $0.7 \times V_{CC}$  on SCL to 50% I/O ( $P_n$ ) output.
- C. All inputs are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

**Figure 21. P-Port Load Circuit and Voltage Waveforms**

## 8 Detailed Description

### 8.1 Overview

The TCA9534 is an 8-bit I/O expander for the two-line bidirectional bus (I<sup>2</sup>C) is designed for 1.65-V to 5.5-V  $V_{CC}$  operation. It provides general-purpose remote I/O expansion for most micro-controller families through the I<sup>2</sup>C interface (serial clock, SCL, and serial data, SDA, pins).

The TCA9534 open-drain interrupt ( $\overline{INT}$ ) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed. The  $\overline{INT}$  pin can be connected to the interrupt input of a micro-controller. By sending an interrupt signal on this line, the remote I/O can inform the micro-controller if there is incoming data on its ports without having to communicate through the I<sup>2</sup>C bus. Thus, the TCA9534 can remain a simple slave device. The device outputs (latched) have high-current drive capability for directly driving LEDs.

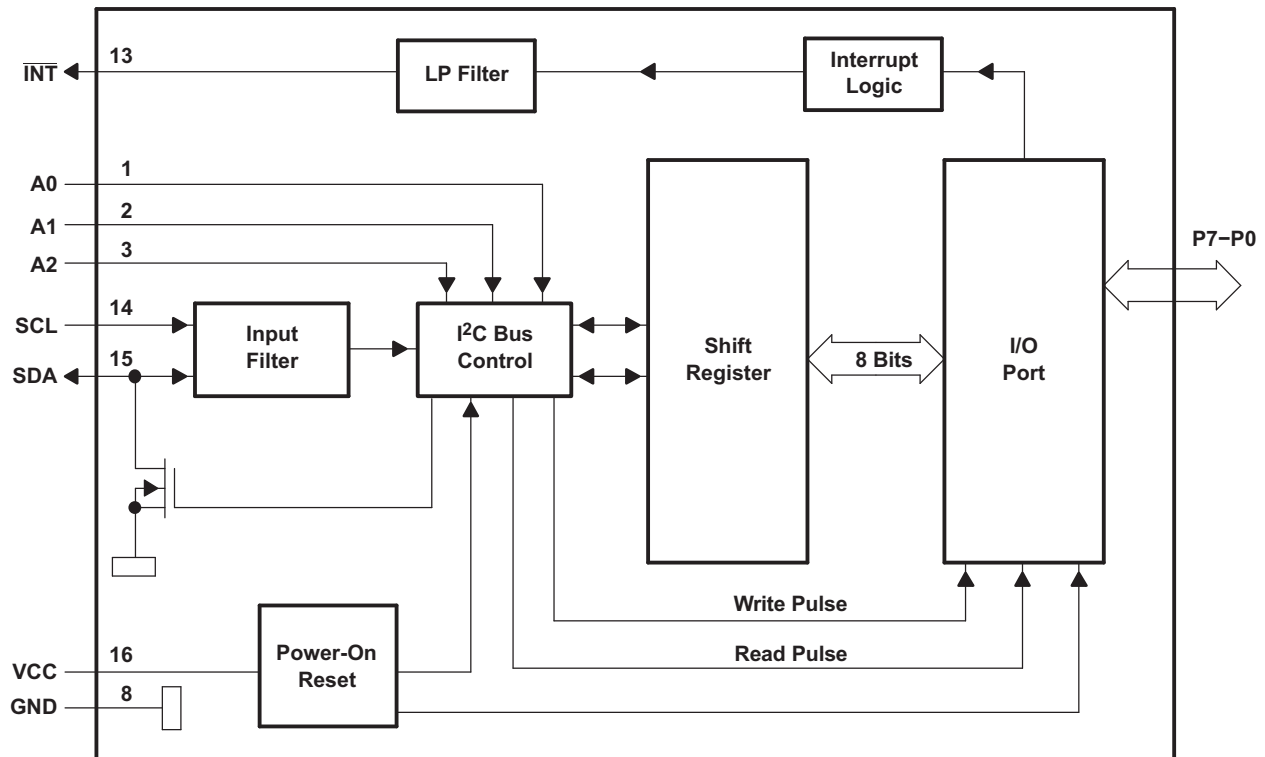
Three hardware pins (A0, A1, and A2) are used to program and vary the fixed I<sup>2</sup>C slave address and allow up to eight devices to share the same I<sup>2</sup>C bus or SMBus.

The system master can reset the TCA9534 in the event of a timeout or other improper operation by cycling the power supply and causing a power-on reset (POR). A reset puts the registers in their default state and initializes the I<sup>2</sup>C/SMBus state machine.

The TCA9534 consists of one 8-bit Configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active high or active low) registers. At power on, the I/Os are configured as inputs. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input Port or Output Port register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

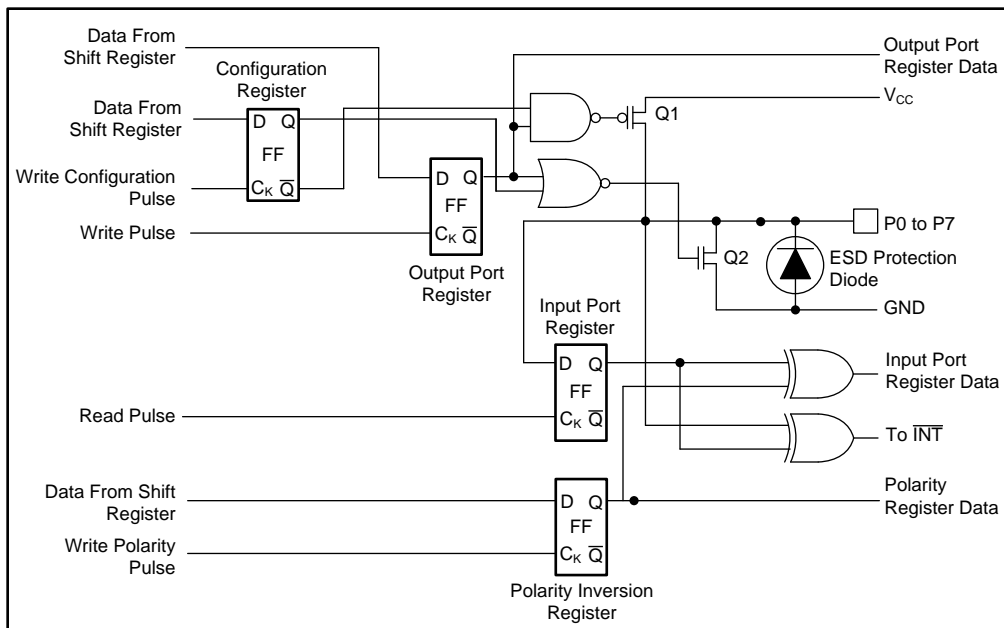
The TCA9534 is identical to the TCA9554 except for the removal of the internal I/O pullup resistors, which greatly reduces power consumption when the I/Os are held LOW.

## 8.2 Functional Block Diagram



Pin numbers shown are for the PW package.

Figure 22. Functional Block Diagram



At power-on reset, all registers return to default values.

Figure 23. Simplified Schematic Of P0 To P7



## 8.3 Feature Description

### 8.3.1 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input. The input voltage may be raised above  $V_{CC}$  to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled depending on the state of the output port register. In this case, there are low impedance paths between the I/O pin and either  $V_{CC}$  or GND. The external voltage applied to this I/O pin must not exceed the recommended levels for proper operation.

### 8.3.2 Interrupt Output ( $\overline{INT}$ )

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time,  $t_{iv}$ , the signal  $\overline{INT}$  is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) bit after the rising edge of the SCL signal. Note that the  $\overline{INT}$  is reset at the ACK just before the byte of changed data is sent. Interrupts that occur during the ACK clock pulse can be lost (or be very short) because of the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as  $\overline{INT}$ .

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

The  $\overline{INT}$  output has an open-drain structure and requires pullup resistor to  $V_{CC}$ .

## 8.4 Device Functional Modes

### 8.4.1 Power-On Reset

When power (from 0 V) is applied to  $V_{CC}$ , an internal power-on reset holds the TCA9534 in a reset condition until  $V_{CC}$  has reached  $V_{PORR}$ . At that point, the reset condition is released and the TCA9534 registers and SMBus/I<sup>2</sup>C state machine initializes to their default states. After that,  $V_{CC}$  must be lowered to below  $V_{PORF}$  and then back up to the operating voltage for a power-on reset cycle.

## 8.5 Programming

### 8.5.1 I<sup>2</sup>C Interface

The TCA9534 has a standard bidirectional I<sup>2</sup>C interface that is controlled by a master device in order to be configured or read the status of this device. Each slave on the I<sup>2</sup>C bus has a specific device address to differentiate between other slave devices that are on the same I<sup>2</sup>C bus. Many slave devices require configuration upon startup to set the behavior of the device. This is typically done when the master accesses internal register maps of the slave, which have unique register addresses. A device can have one or multiple registers where data is stored, written, or read. For more information see the [Understanding the I<sup>2</sup>C Bus](#) application report.

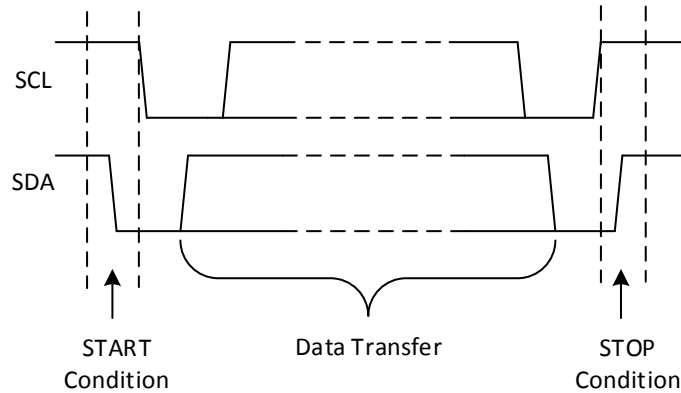
The physical I<sup>2</sup>C interface consists of the serial clock (SCL) and serial data (SDA) lines. Both SDA and SCL lines must be connected to  $V_{CC}$  through a pullup resistor. The size of the pullup resistor is determined by the amount of capacitance on the I<sup>2</sup>C lines. For further details, see the [I<sup>2</sup>C Pullup Resistor Calculation](#) application report. Data transfer may be initiated only when the bus is idle. A bus is considered idle if both SDA and SCL lines are high after a STOP condition.

[Figure 24](#) and [Figure 25](#) show the general procedure for a master to access a slave device:

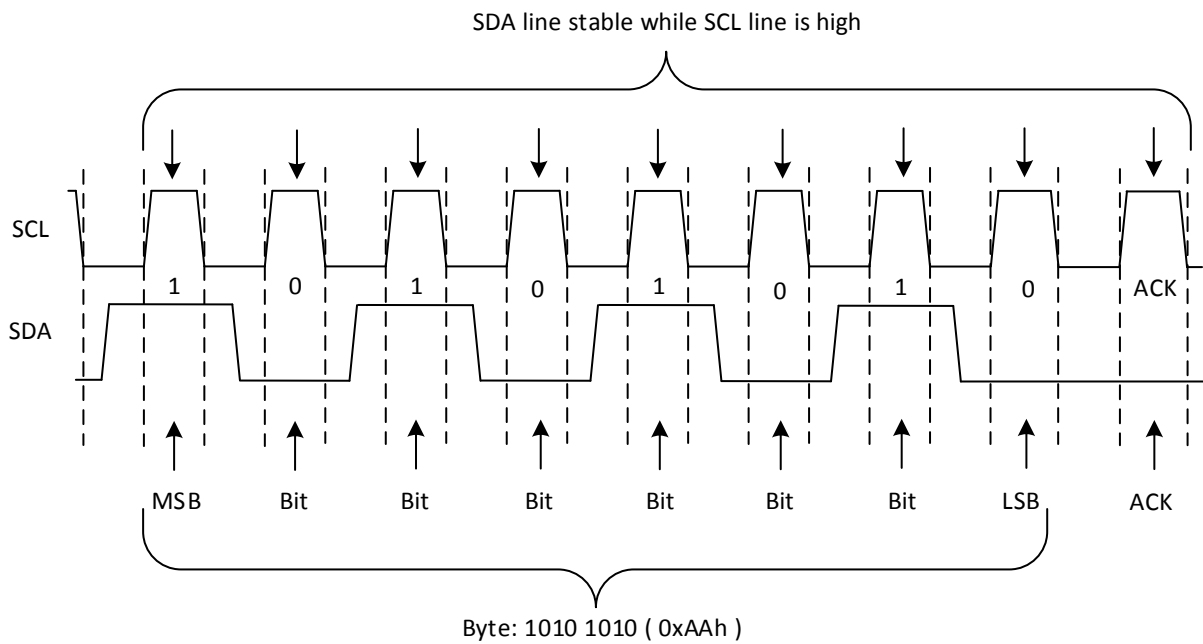
1. If a master wants to send data to a slave:
  - Master-transmitter sends a START condition and addresses the slave-receiver.
  - Master-transmitter sends data to slave-receiver.
  - Master-transmitter terminates the transfer with a STOP condition.
2. If a master wants to receive or read data from a slave:
  - Master-receiver sends a START condition and addresses the slave-transmitter.
  - Master-receiver sends the requested register to read to slave-transmitter.
  - Master-receiver receives data from the slave-transmitter.

**Programming (continued)**

- Master-receiver terminates the transfer with a STOP condition.



**Figure 24. Definition of Start and Stop Conditions**



**Figure 25. Bit Transfer**

Table 1 shows the TCA9534 interface definition.

**Table 1. Interface Definition Table**

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I <sup>2</sup> C slave address	L	H	L	L	A2	A1	A0	R/W
Px I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

## 8.6 Register Maps

### 8.6.1 Device Address

Figure 26 shows the address byte of the TCA9534.

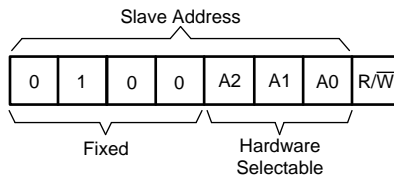


Figure 26. TCA9534 Address

Table 2 shows the TCA9534 address reference.

Table 2. Address Reference

INPUTS			I <sup>2</sup> C BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	32 (decimal), 20 (hexadecimal)
L	L	H	33 (decimal), 21 (hexadecimal)
L	H	L	34 (decimal), 22 (hexadecimal)
L	H	H	35 (decimal), 23 (hexadecimal)
H	L	L	36 (decimal), 24 (hexadecimal)
H	L	H	37 (decimal), 25 (hexadecimal)
H	H	L	38 (decimal), 26 (hexadecimal)
H	H	H	39 (decimal), 27 (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. When it is high (1), a read is selected, while a low (0) selects a write operation.

### 8.6.2 Control Register and Command Byte

Following the successful Acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the TCA9534 (see Figure 27). Two bits of this command byte state the operation (read or write) and the internal register (input, output, polarity inversion or configuration) that is affected. This register can be written or read through the I<sup>2</sup>C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.

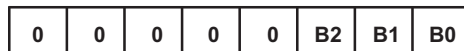


Figure 27. Control Register Bits

Table 3 shows the TCA9534 command byte.

Table 3. Command Byte Table

CONTROL REGISTER BITS		COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B1	B0				
0	0	0x00	Input Port	Read byte	XXXX XXXX
0	1	0x01	Output Port	Read/write byte	1111 1111
1	0	0x02	Polarity Inversion	Read/write byte	0000 0000
1	1	0x03	Configuration	Read/write byte	1111 1111

### 8.6.3 Register Descriptions

The Input Port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level. See [Table 4](#).

Before a read operation, a write transmission is sent with the command byte to indicate to the I<sup>2</sup>C device that the Input Port register is accessed next.

**Table 4. Register 0 (Input Port Register) Table**

BIT	I7	I6	I5	I4	I3	I2	I1	I0
DEFAULT	X	X	X	X	X	X	X	X

The Output Port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value. See [Table 5](#).

**Table 5. Register 1 (Output Port Register) Table**

BIT	O7	O6	O5	O4	O3	O2	O1	O0
DEFAULT	1	1	1	1	1	1	1	1

The Polarity Inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin original polarity is retained. See [Table 6](#).

**Table 6. Register 2 (Polarity Inversion Register) Table**

BIT	N7	N6	N5	N4	N3	N2	N1	N0
DEFAULT	0	0	0	0	0	0	0	0

The Configuration register (register 3) configures the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output. See [Table 7](#).

**Table 7. Register 3 (Configuration Register) Table**

BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	1	1	1	1	1	1	1	1

### 8.6.3.1 Bus Transactions

Data is exchanged between the master and the TCA9534 through write and read commands.

#### 8.6.3.1.1 Writes

To write on the I<sup>2</sup>C bus, the master sends a START condition on the bus with the address of the slave, as well as the last bit (the R/W bit) set to 0, which signifies a write. After the slave sends the acknowledge bit, the master then sends the register address of the register to which it is designated to write. The slave acknowledges again, letting the master know it is ready. After this, the master starts sending the register data to the slave until the master has sent all the data necessary (which is sometimes only a single byte), and the master terminates the transmission with a STOP condition.

See Table 3 to see list of the internal registers and a description of each one.

Figure 28 shows an example of writing a single byte to a slave register.

- Master controls SDA line
- Slave controls SDA line

#### Write to one register in a device

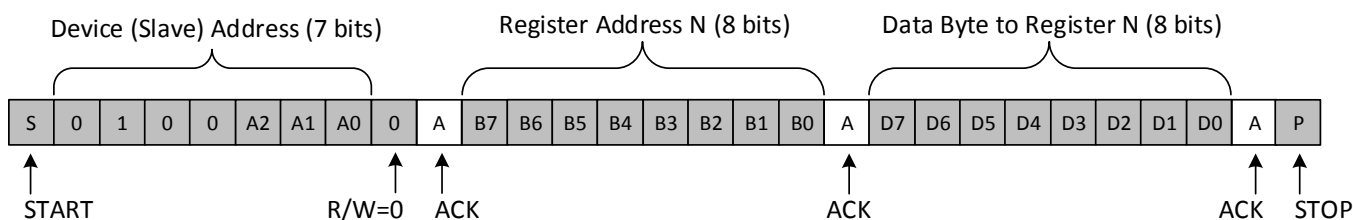


Figure 28. Write to Register

Figure 29 shows an example of writing to the output port register.

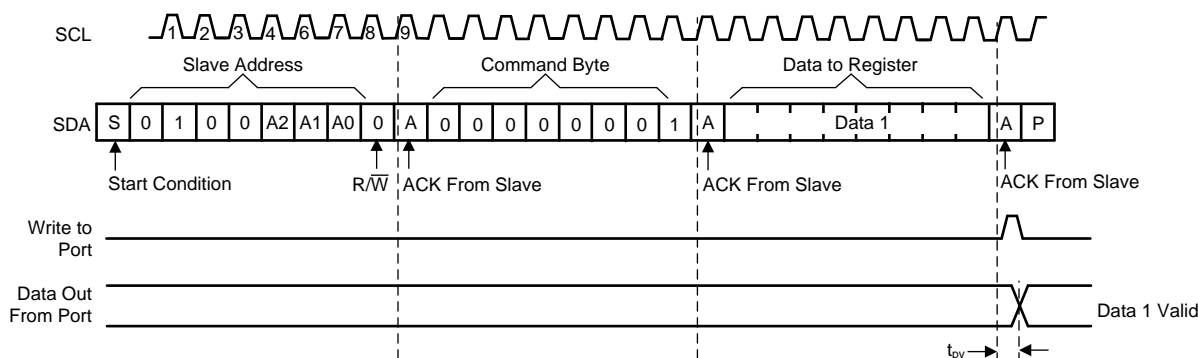


Figure 29. Write to Output Port Register

Figure 30 shows an example of writing to the configuration or polarity inversion registers.

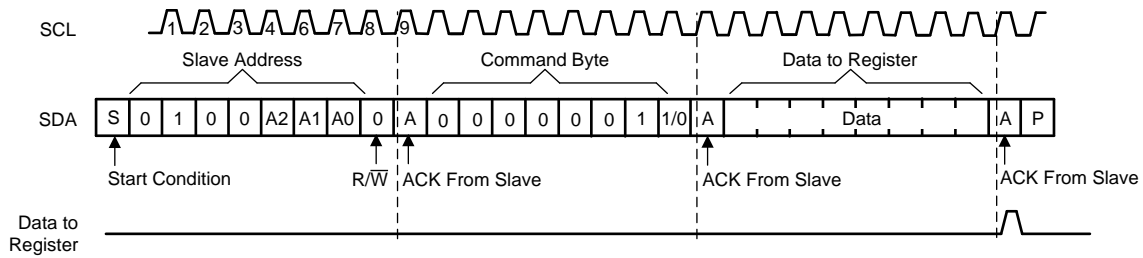


Figure 30. Write to Configuration or Polarity Inversion Registers

8.6.3.1.2 Reads

Reading from a slave is very similar to writing, but requires some additional steps. To read from a slave, the master must first instruct the slave which register it is designated to read from. This is done by the master starting off the transmission in a similar fashion as the write, by sending the address with the R/W bit equal to 0 (signifying a write), followed by the register address it is designated to read from. When the slave acknowledges this register address, the master sends a START condition again, followed by the slave address with the R/W bit set to 1 (signifying a read). This time, the slave acknowledges the read request, and the master releases the SDA bus but continues supplying the clock to the slave. During this part of the transaction, the master becomes the master-receiver, and the slave becomes the slave-transmitter.

The master continues to send out the clock pulses but releases the SDA line so that the slave can transmit data. At the end of every byte of data, the master sends an ACK to the slave, letting the slave know that it is ready for more data. When the master has received the number of bytes it is expecting, it sends a NACK, signaling to the slave to halt communications and release the bus. The master follows this up with a STOP condition.

See Table 3 for the list of the internal registers and a description of each one.

If a read is requested by the master after a POR without first setting the command byte through a write, the device will NACK until a command byte-register address is set as described above.

Figure 31 shows an example of reading a single byte from a slave register.

- Master controls SDA line
- Slave controls SDA line

Read from one register in a device

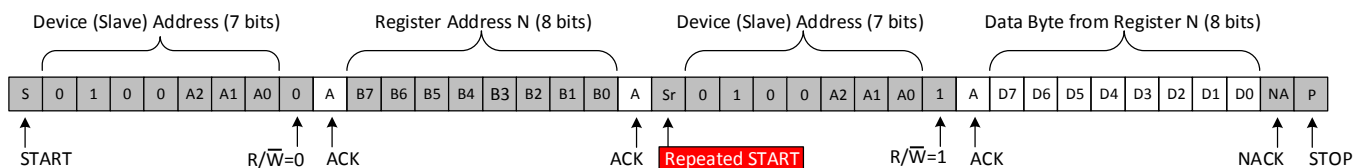
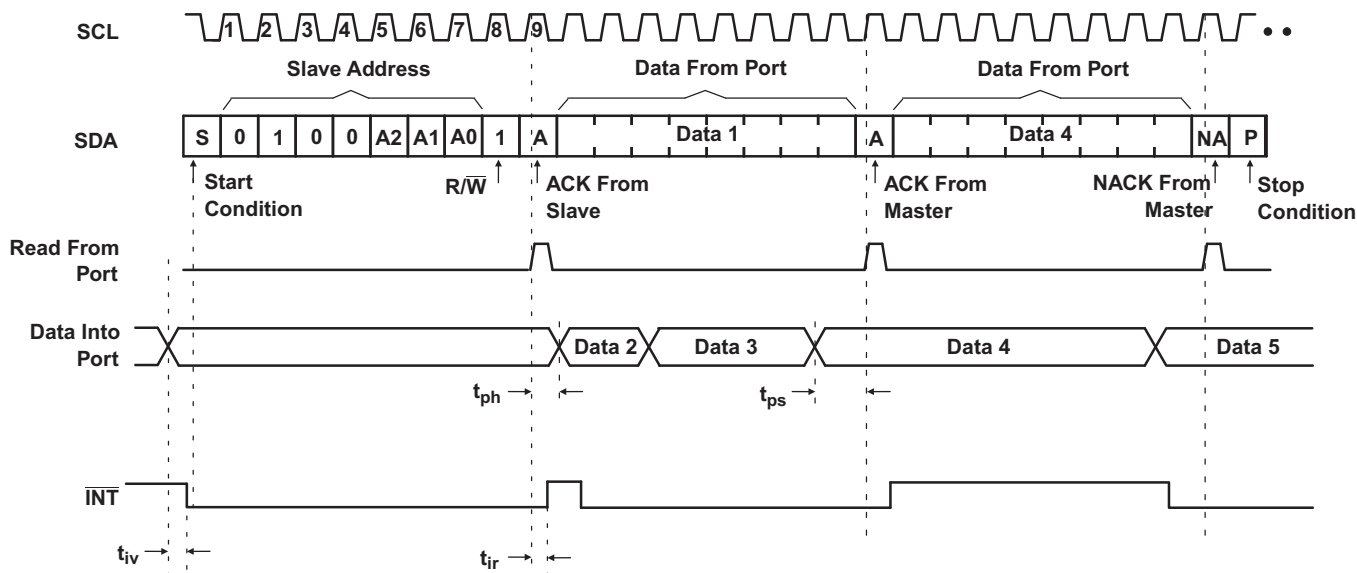


Figure 31. Read from Register

Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data. See Figure 32.



This figure assumes the command byte has previously been programmed with 00h.

Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (Read Input Port register).

This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port (see the [Reads](#) section for these details).

**Figure 32. Read Input Port Register**

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

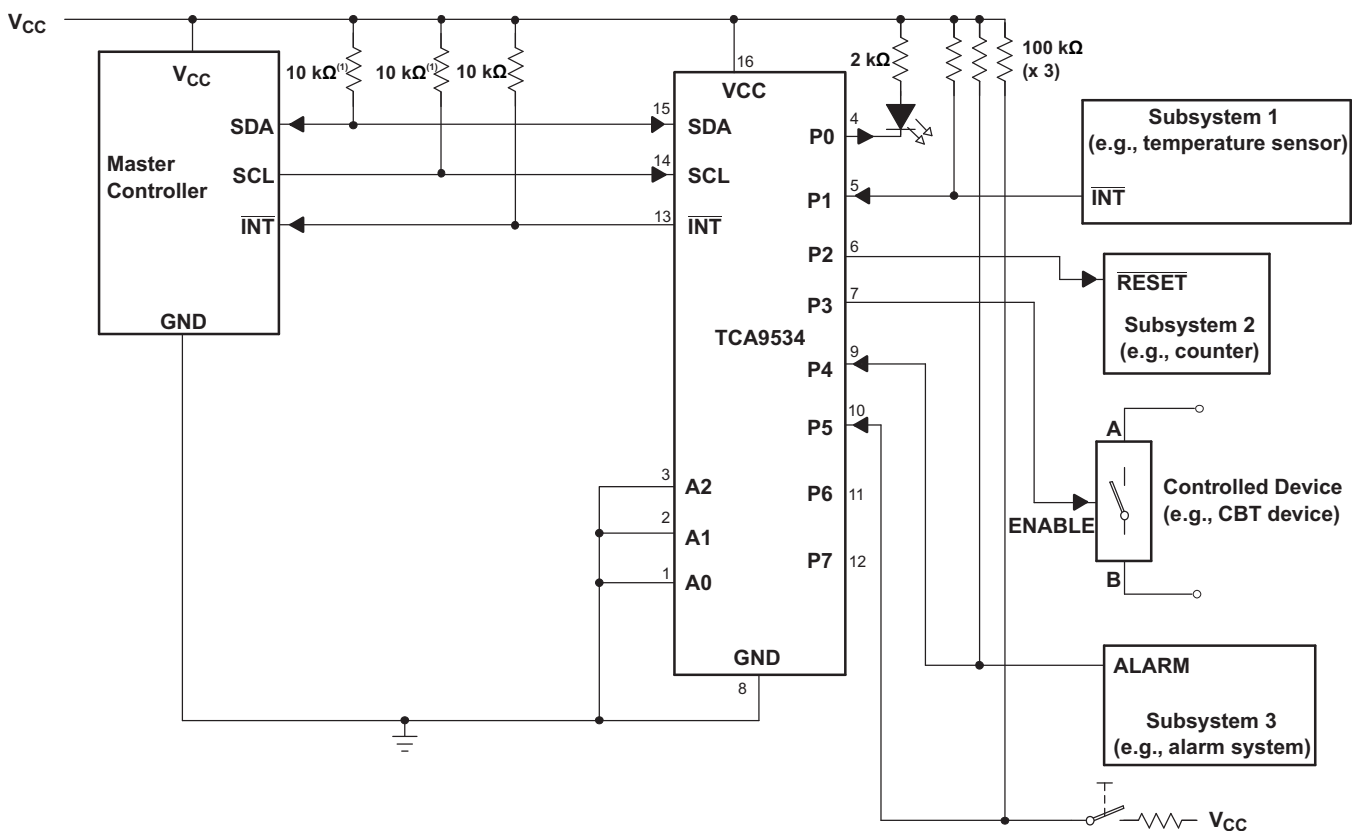
### 9.1 Application Information

Figure 33 shows an application in which the TCA9534 can be used.

I/O Expanders such as the TCA9534 are commonly used to obtain more general purpose I/Os. There are many common uses for these additional I/Os:

- Inputs from other ICs, such as interrupt signals from sensors
- Inputs from physical buttons (for detecting button presses)
- Outputs to control RESET or ENABLE signals on other ICs
- Outputs for controlling LEDs for visual feedback to a user

### 9.2 Typical Application



The SCL and SDA pins must be tied directly to VCC because if SCL and SDA are tied to an auxiliary power supply that could be powered on while VCC is powered off, then the supply current, ICC, will increase as a result.

Device address is configured as 0100000 for this example.

P0, P2, and P3 are configured as outputs.

P1, P4, and P5 are configured as inputs.

P6 and P7 are not used and must be configured as outputs.

**Figure 33. Application Schematic**



## Typical Application (continued)

### 9.2.1 Design Requirements

#### 9.2.1.1 Calculating Junction Temperature and Power Dissipation

When designing with the TCA9534, it is important that the *Recommended Operating Conditions* not be violated. Many of the parameters of this device are rated based on junction temperature. So junction temperature must be calculated in order to verify that safe operation of the device is met. The basic equation for junction temperature is shown in Equation 1.

$$T_j = T_A + (\theta_{JA} \times P_d) \quad (1)$$

$\theta_{JA}$  is the standard junction to ambient thermal resistance measurement of the package, as seen in *Thermal Information* table.  $P_d$  is the total power dissipation of the device, and the approximation is shown in Equation 2.

$$P_d \approx (I_{CC\_STATIC} \times V_{CC}) + \sum P_{d\_PORT\_L} + \sum P_{d\_PORT\_H} \quad (2)$$

Equation 2 is the approximation of power dissipation in the device. The equation is the static power plus the summation of power dissipated by each port (with a different equation based on if the port is outputting high, or outputting low. If the port is set as an input, then power dissipation is the input leakage of the pin multiplied by the voltage on the pin). Note that this ignores power dissipation in the INT and SDA pins, assuming these transients to be small. They can easily be included in the power dissipation calculation by using Equation 3 to calculate the power dissipation in INT or SDA while they are pulling low, and this gives maximum power dissipation.

$$P_{d\_PORT\_L} = (I_{OL} \times V_{OL}) \quad (3)$$

Equation 3 shows the power dissipation for a single port which is set to output low. The power dissipated by the port is the  $V_{OL}$  of the port multiplied by the current it is sinking.

$$P_{d\_PORT\_H} = (I_{OH} \times (V_{CC} - V_{OH})) \quad (4)$$

Equation 4 shows the power dissipation for a single port which is set to output high. The power dissipated by the port is the current sourced by the port multiplied by the voltage drop across the device (difference between  $V_{CC}$  and the output voltage).

#### 9.2.1.2 Minimizing $I_{CC}$ when I/Os Control LEDs

When the I/Os are used to control LEDs, normally, these are connected to  $V_{CC}$  through a resistor as shown in Figure 33. For a P-port configured as an input,  $I_{CC}$  increases as  $V_I$  becomes lower than  $V_{CC}$ . The LED is a diode, with threshold voltage  $V_T$ , and when a P-port is configured as an input the LED is off but  $V_I$  is a  $V_T$  drop below  $V_{CC}$ .

For battery-powered applications, it is essential that the voltage of P-ports controlling LEDs is greater than or equal to  $V_{CC}$  when the P-ports are configured as input to minimize current consumption. Figure 34 shows a high-value resistor in parallel with the LED. Figure 35 shows  $V_{CC}$  less than the LED supply voltage by at least  $V_T$ . Both of these methods maintain the I/O  $V_I$  at or above  $V_{CC}$  and prevents additional supply current consumption when the P-port is configured as an input and the LED is off.

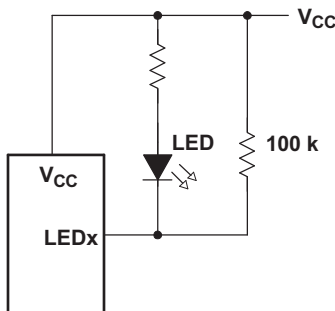


Figure 34. High-Value Resistor in Parallel with LED

Typical Application (continued)

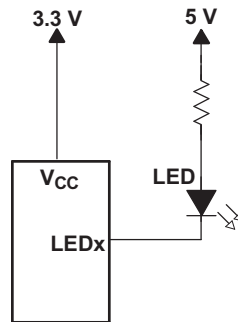


Figure 35. Device Supplied by a Lower Voltage

9.2.2 Detailed Design Procedure

The pullup resistors,  $R_p$ , for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all slaves on the I<sup>2</sup>C bus. The minimum pullup resistance is a function of  $V_{CC}$ ,  $V_{OL(max)}$ , and  $I_{OL}$  as shown in Equation 5.

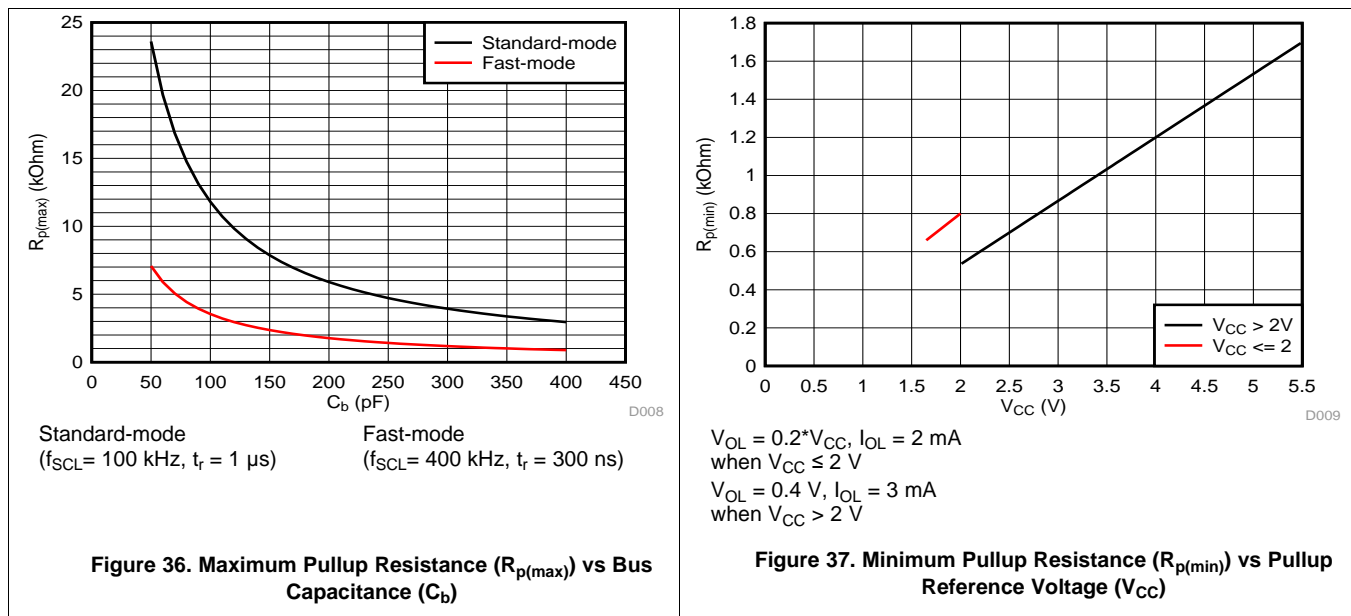
$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \tag{5}$$

The maximum pullup resistance is a function of the maximum rise time,  $t_r$  (300 ns for fast-mode operation,  $f_{SCL} = 400$  kHz) and bus capacitance,  $C_b$  as shown in Equation 6.

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \tag{6}$$

The maximum bus capacitance for an I<sup>2</sup>C bus must not exceed 400 pF for standard mode or fast mode operation. The bus capacitance can be approximated by adding the capacitance of the TCA9534,  $C_i$  for SCL or  $C_{i0}$  for SDA, the capacitance of wires, connections, traces, and the capacitance of additional slaves on the bus.

9.2.3 Application Curves



## 10 Power Supply Recommendations

### 10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, the TCA9534 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device goes through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in [Figure 38](#) and [Figure 39](#).

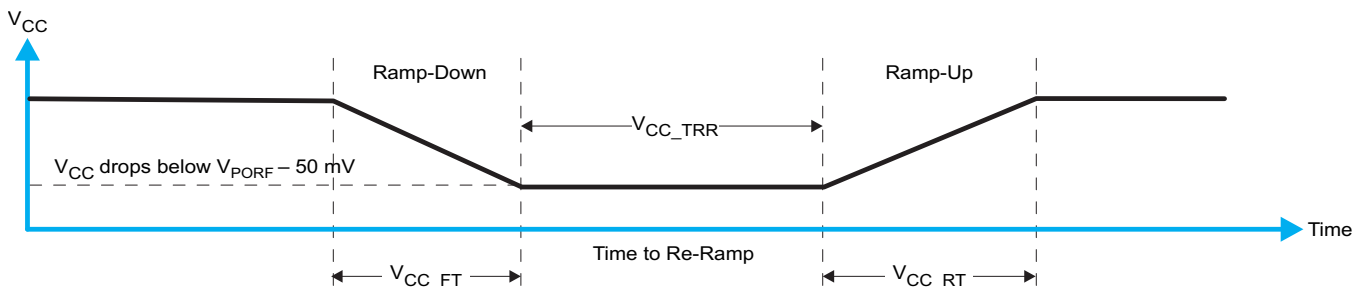


Figure 38.  $V_{CC}$  is Lowered Below the  $P_{ORF}$  Threshold, Then Ramped Back Up to  $V_{CC}$

[Table 8](#) specifies the performance of the power-on reset feature for the TCA9534 for both types of power-on reset.

Table 8. Recommended Supply Sequencing and Ramp Rates<sup>(1)</sup>

PARAMETER			MIN	MAX	UNIT
$V_{CC\_FT}$	Fall rate	See <a href="#">Figure 38</a>	1	2000	ms
$V_{CC\_RT}$	Rise rate	See <a href="#">Figure 38</a>	0.1	2000	ms
$V_{CC\_TRR}$	Time to re-ramp (when $V_{CC}$ drops to $V_{POR\_MIN} - 50$ mV or when $V_{CC}$ drops to GND)	See <a href="#">Figure 38</a>	1		$\mu$ s
$V_{CC\_GH}$	Level that $V_{CCP}$ can glitch down to, but not cause a functional disruption when $V_{CCX\_GW} = 1$ $\mu$ s	See <a href="#">Figure 39</a>		1.2	V
$V_{CC\_MV}$	The minimum voltage that $V_{CC}$ can glitch down to without causing a reset ( $V_{CC\_GH}$ must not be violated)	See <a href="#">Figure 39</a>	1.5		V
$V_{CC\_GW}$	Glitch width that does not cause a functional disruption when $V_{CCX\_GH} = 0.5 \times V_{CCx}$	See <a href="#">Figure 39</a>		10	$\mu$ s

(1) All supply sequencing and ramp rate values are measured at  $T_A = 25^\circ\text{C}$

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ( $V_{CC\_GW}$ ) and height ( $V_{CC\_GH}$ ) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. [Figure 39](#) and [Table 8](#) provide more information on how to measure these specifications.

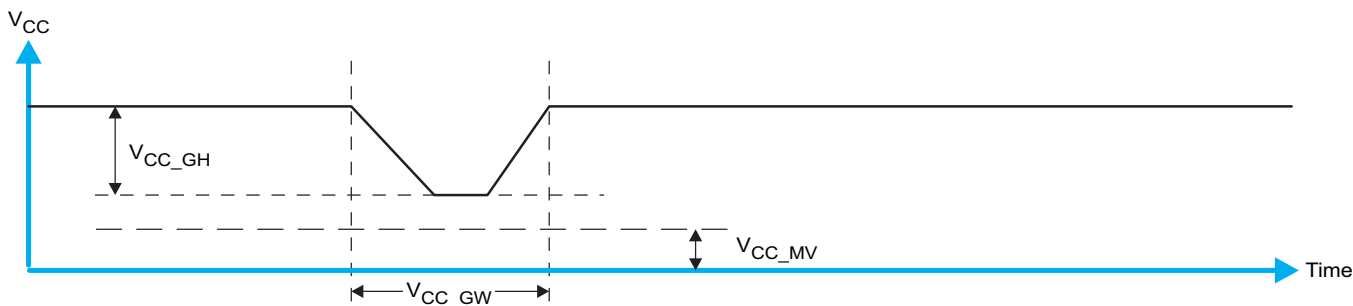
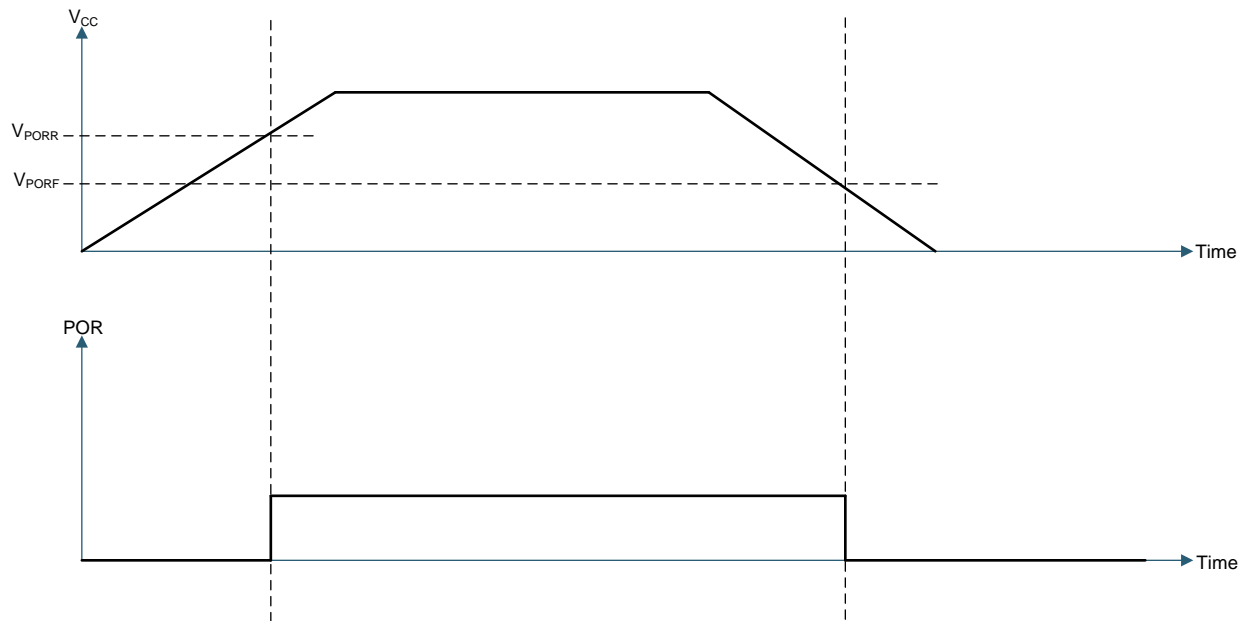


Figure 39. Glitch Width and Glitch Height

$V_{POR}$  is critical to the power-on reset.  $V_{PORR}$  is the voltage level at which the reset condition is released and all the registers and the I<sup>2</sup>C-SMBus state machine are initialized to their default states. The value of  $V_{POR}$  differs based on the  $V_{CC}$  being lowered to or from 0. [Figure 40](#) and [Table 8](#) provide more details on this specification.



**Figure 40.**  $V_{POR}$

## 11 Layout

### 11.1 Layout Guidelines

For printed circuit board (PCB) layout of the TCA9534, common PCB layout practices must be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I<sup>2</sup>C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors must be placed as close to the TCA9534 as possible. These best practices are shown in Figure 41.

For the layout example provided in Figure 41, it must be possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power (V<sub>CC</sub>) and ground (GND). However, a 4-layer board is preferable for boards with higher density signal routing. On a 4-layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to V<sub>CC</sub> or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in Figure 41.

### 11.2 Layout Example

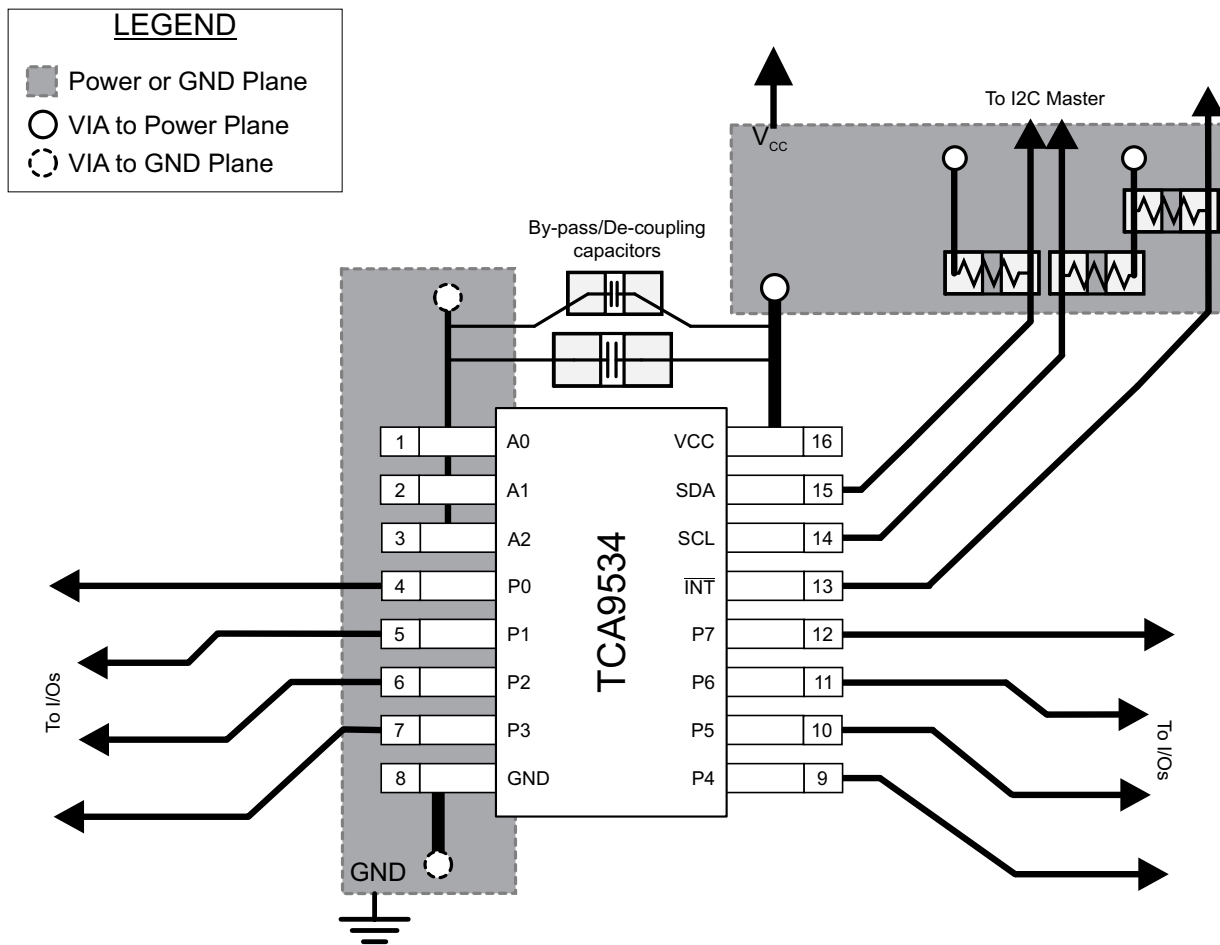


Figure 41. TCA9534 Layout

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

- [I2C Bus Pull-Up Resistor Calculation](#)
- [Maximum Clock Frequency of I2C Bus Using Repeaters](#)
- [Introduction to Logic](#)
- [Understanding the I2C Bus](#)
- [Choosing the Correct I2C Device for New Designs](#)
- [I/O Expander EVM User's Guide](#)

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 Trademarks

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### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.6 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9534DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TCA9534	<a href="#">Samples</a>
TCA9534DWT	ACTIVE	SOIC	DW	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TCA9534	<a href="#">Samples</a>
TCA9534PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW534	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9534DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TCA9534DWT	SOIC	DW	16	250	180.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TCA9534PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9534DWR	SOIC	DW	16	2000	350.0	350.0	43.0
TCA9534DWT	SOIC	DW	16	250	213.0	191.0	55.0
TCA9534PWR	TSSOP	PW	16	2000	356.0	356.0	35.0

## GENERIC PACKAGE VIEW

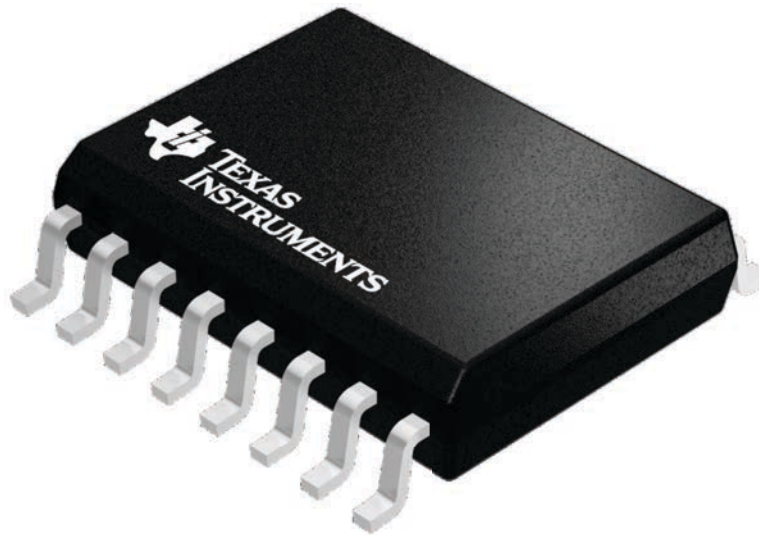
**DW 16**

**SOIC - 2.65 mm max height**

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224780/A

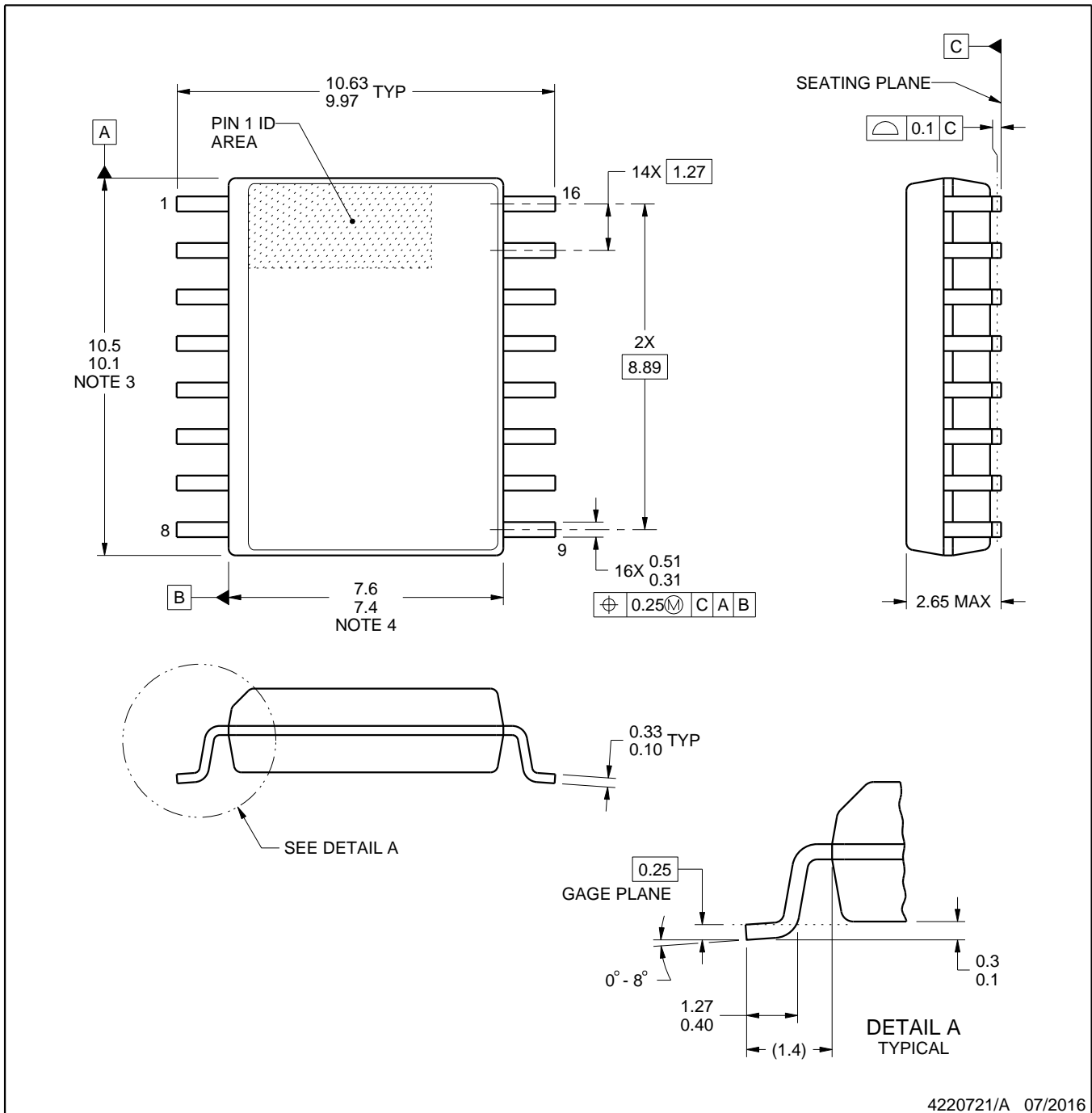


DW0016A

# PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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