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SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

Digital terminal equipments – General

Physical/electrical characteristics of hierarchical digital interfaces

Recommendation ITU-T G.703

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Recommendation ITU-T G.703

Physical/electrical characteristics of hierarchical digital interfaces

Summary

Recommendation ITU-T G.703 specifies the recommended physical and electrical characteristics of the interfaces at hierarchical bit rates as described in Recommendations ITU-T G.702 (PDH) and ITU-T G.707 (SDH). The interfaces are defined in terms of general characteristics, specifications at the output ports and input ports and/or cross-connect points, earthing of outer conductor or screen and coding rules.

History

Edition	Recommendation	Approval	Study Group	Unique ID*
1.0	ITU-T G.703	1972-12-15		11.1002/1000/11264
2.0	ITU-T G.703	1976-10-08		11.1002/1000/9993
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6.0	ITU-T G.703	1991-04-05	XVIII	11.1002/1000/895
7.0	ITU-T G.703	1998-10-13	15	11.1002/1000/4514
8.0	ITU-T G.703	2001-11-29	15	11.1002/1000/5602
8.1	ITU-T G.703 (2001) Cor. 1	2008-03-29	15	11.1002/1000/9369
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Keywords

Electrical interface, PDH, plesiochronous digital hierarchy, SDH, synchronous digital hierarchy, synchronization interface.

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FOREWORD

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The World Telecommunication Standardization Assembly (WTSA), which meets every four years, establishes the topics for study by the ITU-T study groups which, in turn, produce Recommendations on these topics.

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In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

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As of the date of approval of this Recommendation, ITU had not received notice of intellectual property, protected by patents, which may be required to implement this Recommendation. However, implementers are cautioned that this may not represent the latest information and are therefore strongly urged to consult the TSB patent database at http://www.itu.int/ITU-T/ipr/.

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Recommendation ITU-T G.703

Physical/electrical characteristics of hierarchical digital interfaces

1 Scope

This Recommendation provides the recommended physical and electrical characteristics of the interfaces at hierarchical bit rates as described in [ITU-T G.702] (PDH) and [ITU-T G.707] (SDH), to enable the interconnection of digital network components (digital sections, multiplex equipment, exchanges) to form an international digital link or connection. The characteristics given in this Recommendation should be applied to new equipment (component) designs.

NOTE 1 – The characteristics of interfaces at non-hierarchical bit rates, except $n \times 64$ kbit/s interfaces conveyed by 1544 kbit/s or 2048 kbit/s interfaces and 3152 kbit/s interface in North American hierarchy, are specified in the respective equipment Recommendations.

NOTE 2 – The jitter specifications contained in this Recommendation are intended to be imposed at international interconnection points.

NOTE 3 – The interfaces described in clauses 5 to 12 correspond to the ports T (output port) and T′ (input port) as recommended for interconnection in [b-ITU-R F.596-1] (Interconnection of digital radio-relay systems).

NOTE 4 – For signals with bit rates of $n \times 64$ kbit/s (n = 2 to 31) which are routed through multiplexing equipment specified for the 2048 kbit/s hierarchy, the interface shall have the same physical/electrical characteristics as those for the 2048 kbit/s interface specified in clause 9. For signals with bit rates of $n \times 64$ kbit/s (n = 2 to 23) which are routed through multiplexing equipment specified for the 1544 kbit/s hierarchy, the interface shall have the same physical/electrical characteristics as those for the 1544 kbit/s interface specified in clause 5.

NOTE 5 – The specifications contained in this Recommendation are related to the physical interface only (i.e., to characterize the line codes and input/output equipment interfaces); in particular, the required frequency tolerances do not imply overall equipment performances which may be driven by tighter requirements in Recommendations for specific network/equipment applications (e.g., [ITU-T G.813] and [b-ITU-T G.783]).

NOTE 6 – When measuring the performance of the output port described in clauses 6.2.1.2, 11.2, 12.2, 13.2, 14.2, 15.2, 17.2, 18.2, and 20.2, the signal attenuation, signal distortion, and length of the cable should be as small as possible. The length of the cable used could be chosen to be less than three meters, for example.

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published. The reference to a document within this Recommendation does not give it, as a stand-alone document, the status of a Recommendation.

[ITU-T G.701] Recommendation ITU-T G.701 (1993), *Vocabulary of digital transmission and multiplexing, and pulse code modulation (PCM) terms*.

[ITU-T G.702] Recommendation ITU-T G.702 (1988), *Digital hierarchy bit rates*.

[ITU-T G.704] Recommendation ITU-T G.704 (1998), *Synchronous frame structures used at 1544, 6312, 2048, 8448 and 44 736 kbit/s hierarchical levels*.

[ITU-T G.707] Recommendation ITU-T G.707/Y.1322 (2007), *Network node interface for the synchronous digital hierarchy (SDH)*.

[ITU-T G.742] Recommendation ITU-T G.742 (1988), *Second order digital multiplex equipment operating at 8448 kbit/s and using positive justification*.

[ITU-T G.747] Recommendation ITU-T G.747 (1988), *Second order digital multiplex equipment operating at 6312 kbit/s and multiplexing three tributaries at 2048 kbit/s*.

[ITU-T G.751] Recommendation ITU-T G.751 (1988), *Digital multiplex equipments operating at the third order bit rate of 34 368 kbit/s and the fourth order bit rate of 139 264 kbit/s and using positive justification*.

[ITU-T G.752] Recommendation ITU-T G.752 (1988), *Characteristics of digital multiplex equipments based on a second order bit rate of 6312 kbit/s and using positive justification*.

[ITU-T G.753] Recommendation ITU-T G.753 (1988), *Third order digital multiplex equipment operating at 34 368 kbit/s and using positive/zero/ negative justification*.

[ITU-T G.755] Recommendation ITU-T G.755 (1988), *Digital multiplex equipment operating at 139 264 kbit/s and multiplexing three tributaries at 44 736 kbit/s*.

[ITU-T G.810] Recommendation ITU-T G.810 (1996), Definitions and terminology for synchronization networks.

[ITU-T G.811] Recommendation ITU-T G.811 (1997), *Timing characteristics of primary reference clocks*.

[ITU-T G.812] Recommendation ITU-T G.812 (2004), *Timing requirements of slave clocks suitable for use as node clocks in synchronization networks*.

[ITU-T G.813] Recommendation ITU-T G.813 (2003), *Timing characteristics of SDH equipment slave clocks (SEC)*.

[ITU-T G.823] Recommendation ITU-T G.823 (2000), *The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy*.

[ITU-T G.824] Recommendation ITU-T G.824 (2000), *The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy*.

[ITU-T G.825] Recommendation ITU-T G.825 (2000), *The control of jitter and wander within digital networks which are based on the synchronous digital hierarchy (SDH)*.

[ITU-T G.8260] Recommendation ITU-T G.8260 (2015), *Definitions and terminology for synchronization in packet networks*.

[ITU-T G.8271] Recommendation ITU-T ITU-T G.8271/Y.1366 (2012), *Time and phase synchronization aspects of packet networks*.

[ITU-T G.8272] Recommendation ITU-T G.8272/Y.1367 (2015), *Timing characteristics of primary reference time clocks.*

[ITU-T K.20] Recommendation ITU-T K.20 (2015), *Resistibility of telecommunication equipment installed in a telecommunication centre to overvoltages and overcurrents*.

[ITU-T K.27] Recommendation ITU-T K.27 (2015), *Bonding configurations and earthing inside a telecommunication building*.

[ITU-T O.151] Recommendation ITU-T O.151 (1992), *Error performance measuring equipment operating at the primary rate and above*.

[ITU-T O.172] Recommendation ITU-T O.172 (2005), *Jitter and wander measuring equipment for digital systems which are based on the synchronous digital hierarchy (SDH)*.

[ITU-T V.11] Recommendation ITU-T ITU-T V.11 (1996), *Electrical characteristics for balanced double-current interchange circuits operating at data signalling rates up to 10 Mbit/s.*

[ITU-R F.750-4] Recommendation ITU-R F.750-4 (2000), *Architectures and functional aspects of radio-relay systems for synchronous digital hierarchy (SDH)–-based networks*.

[IEC 60469] IEC 60469 (2013), *Transitions, pulses and related waveforms – Terms, definitions and algorithms*.

[IEC 60469-2] IEC 60469-2 (1987), *Pulse techniques and apparatus – Part 2: Pulse measurement and analysis, general considerations*.

[IEC 60603-7] IEC 60603-7 ed3.1 Consol. with am1 (2011), *Connectors for electronic equipment – Part 7: Detail specification for 8-way, unshielded, free and fixed connectors*.

[ETSI ETS 300 166] ETSI ETS 300 166 (1993), *Transmission and Multiplexing (TM); Physical and electrical characteristics of hierarchical digital interfaces for equipment using the 2048 kbit/s-based plesiochronous or synchronous digital hierarchies*.

3 Definitions

3.1 Terms defined elsewhere

This Recommendation uses the following terms defined elsewhere:

3.1.1 (timing) jitter [ITU-T G.810].

3.1.2 time synchronization [ITU-T G.8260].

3.2 Terms defined in this Recommendation

None.

4 Abbreviations and acronyms

This Recommendation uses the following abbreviations and acronyms:

1PPS One Pulse Per Second

AIS Alarm Indication Signal

AMI Alternate Mark Inversion

B3ZS Bipolar with three-Zero Substitution

B8ZS Bipolar with eight-Zero Substitution

CMI Coded Mark Inversion

DC Direct Current

DSN Digital Switching Network

EMC Electromagnetic Compatibility

EPRTC Enhanced Primary Reference Time Clock

GND Ground

GNSS Global Navigation Satellite System

HDB2 High Density Bipolar of order 2 code

HDB3 High Density Bipolar of order 3 code

PCM Pulse Code Modulation

PRBS Pseudo Random Bit Sequence

PRC Primary Reference Clock

PRTC Primary Reference Time Clock

PDH Plesiochronous Digital Hierarchy

SDH Synchronous Digital Hierarchy

SEC SDH Equipment Clock

SSU Synchronization Supply Unit

STM Synchronous Transport Module

ZBTSI Zero Byte Time Slot Interchange

5 Conventions

None.

6 Interface at 64 kbit/s (E0)

6.1 Functional requirements

The following basic requirements for the design of the interface are recommended.

In both directions of transmission, three signals can be carried across the interface:

– 64 kbit/s information signal;

– 64 kHz timing signal;

– 8 kHz timing signal.

NOTE 1 – The 64 kbit/s information signal and the 64 kHz timing signal are mandatory. However, although an 8 kHz timing must be generated by the controlling equipment (e.g., PCM multiplex or time slot access equipment), it should not be mandatory for the subordinate equipment on the other side of the interface to either utilize the 8 kHz timing signal from the controlling equipment or to supply an 8 kHz timing signal.

NOTE 2 – The detection of an upstream fault can be transmitted across the 64 kbit/s interface by transmitting an alarm indication signal (AIS) towards the subordinate equipment.

The interface should be bit sequence independent at 64 kbit/s.

NOTE 3 – An unrestricted 64 kbit/s signal can be transmitted across the interface. However, this does not imply that unrestricted 64 kbit/s paths are realizable on a global basis. This is because some Administrations presently have or are continuing to install extensive networks composed of digital line sections whose characteristics do not permit the transmission of long sequences of 0s. [b-ITU-T G.733] provides for PCM multiplexes with characteristics appropriate for such digital line sections.) Specifically, for octet timed sources in 1544 kbit/s digital networks, it is required that at least one binary 1 should be contained in any octet of a 64 kbit/s digital signal. For a bit stream which is not octet-timed, no more than 7 consecutive 0s should appear in the 64 kbit/s signal.

NOTE 4 – Although the interface is bit sequence independent, the use of the AIS (all 1s bit pattern) may result in some minor restrictions for the 64 kbit/s source. For example, an all 1s alignment signal could result in problems.

6.1.1 Three types of envisaged interfaces

6.1.1.1 Codirectional interface

The term "codirectional" is used to describe an interface across which the information and its associated timing signal are transmitted in the same direction (see Figure 6-1).

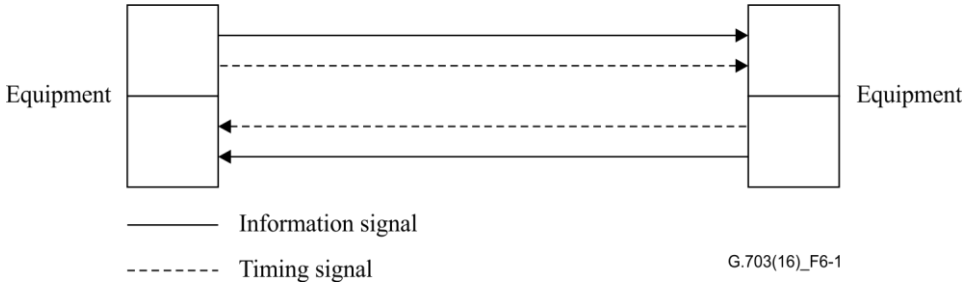


Figure 6-1 – Codirectional interface

6.1.1.2 Centralized clock interface

The term "centralized clock" is used to describe an interface wherein for both directions of transmission of the information signal, the associated timing signals are supplied from a centralized clock, which may be derived for example from certain incoming line signals (see Figure 6-2).

NOTE – The codirectional interface or centralized clock interface should be used for synchronized networks and for plesiochronous networks having clocks of the stability required (see [ITU-T G.811]) to ensure an adequate interval between the occurrence of slips.

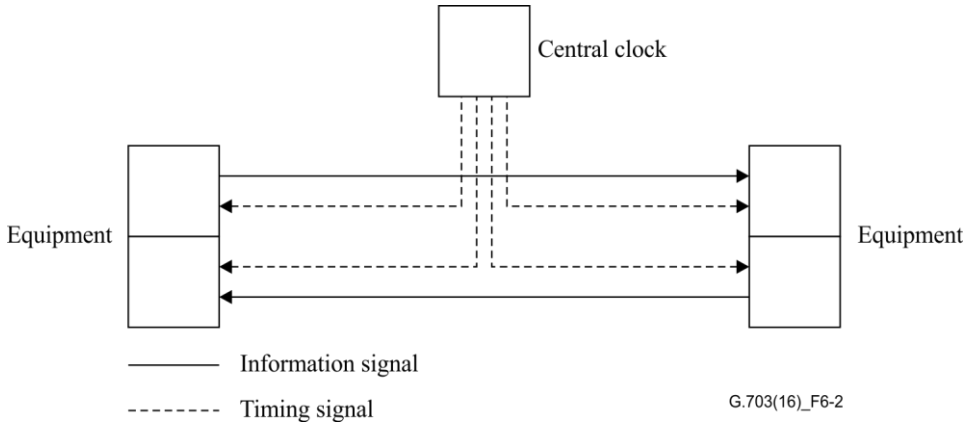


Figure 6-2 – Centralized clock interface

6.1.1.3 Contradirectional interface

The term "contradirectional" is used to describe an interface across which the timing signals associated with both directions of transmission are directed towards the subordinate equipment (see Figure 6-3).

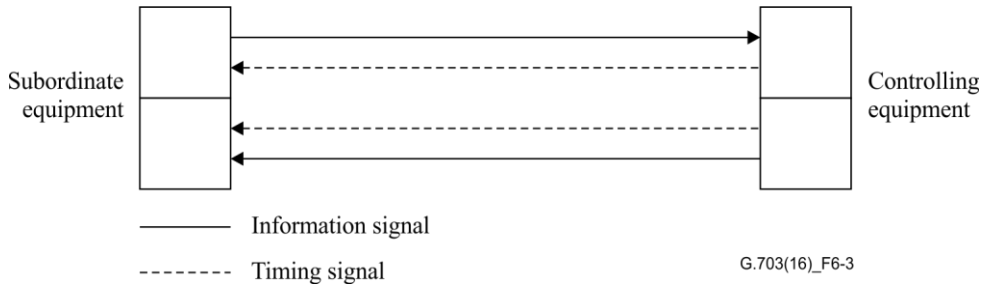


Figure 6-3 – Contradirectional interface

6.2 Electrical characteristics

6.2.1 Electrical characteristics of 64 kbit/s codirectional interface

6.2.1.1 General characteristics

Nominal bit rate: 64 kbit/s.

Bit rate accuracy: ±100 ppm (±6.4 bit/s) or better.

64 kHz and 8 kHz timing signal to be transmitted in a codirectional way with the information signal.

One balanced pair for each direction of transmission; the use of transformers is recommended.

Code conversion rules:

Step 1 – A 64 kbit/s bit period is divided into four unit intervals.

Step 2 – A binary one is coded as a block of the following four bits:

1 1 0 0

Step 3 – A binary zero is coded as a block of the following four bits:

1 0 1 0

Step 4 – The binary signal is converted into a three-level signal by alternating the polarity of consecutive blocks.

Step 5 – The alternation in polarity of the blocks is violated every 8th block. The violation block marks the last bit in an octet.

These conversion rules are illustrated in Figure 6-4.

Overvoltage protection requirements: refer to [ITU-T K.20].

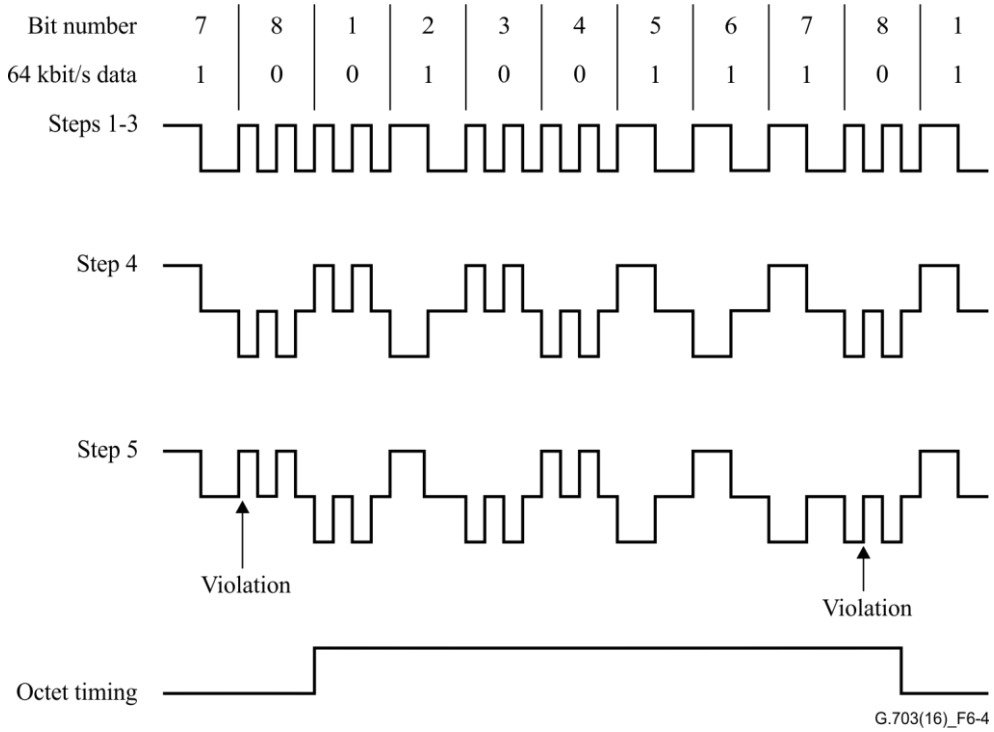


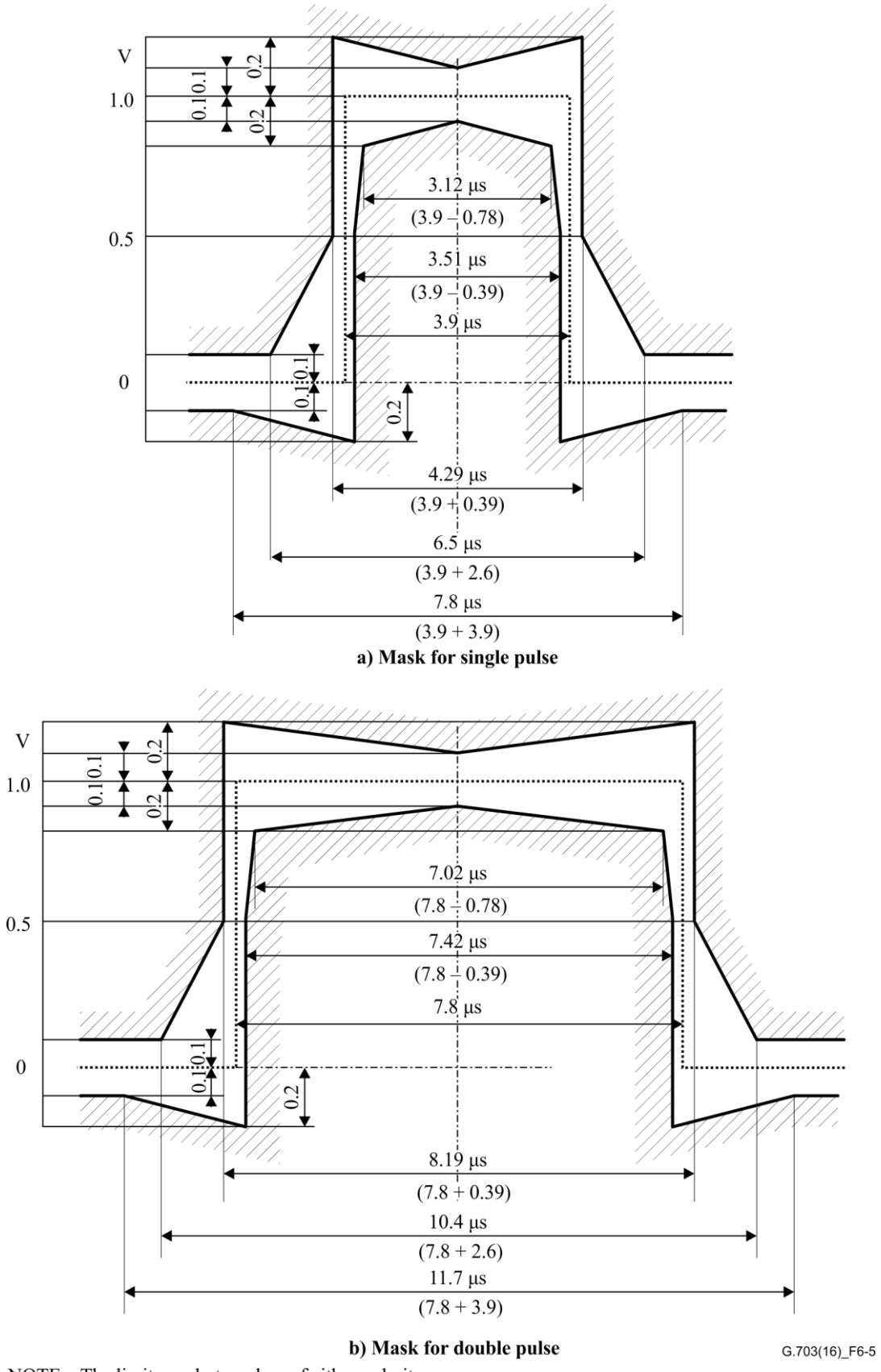
Figure 6-4 – Illustration of the conversion rules

6.2.1.2 Specifications at the output ports

See Table 6-1. See also Note 6 of clause 1.

Table 6-1 – Digital 64 kbit/s codirectional interface

Symbol rate	256 kBauds
Pulse shape (nominally rectangular)	All pulses of a valid signal must conform to the masks in Figure 6-5, irrespective of the polarity
Pair for each direction	One symmetric pair
Test load impedance	120 ohms resistive
Nominal peak voltage of a "mark" (pulse)	1.0 V
Peak voltage of a "space" (no pulse)	0 V ± 0.10 V
Nominal pulse width	3.9 μs
Ratio of the amplitudes of positive and negative pulses at the centre of the pulses interval	0.95 to 1.05
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05
Maximum peak-to-peak jitter at the output port (Note)	Refer to clause 5.1 of [ITU-T G.823]
NOTE – For the time being these values are valid only for equipment of the 2 Mbit/s hierarchy.	



NOTE – The limits apply to pulses of either polarity.

Figure 6-5 – Pulse masks of the 64 kbit/s codirectional interface

The return loss at the output port should have the minimum values given in Table 6-2:

Table 6-2 – Digital 64 kbit/s codirectional interface output port minimum return loss

Frequency range (kHz)	Return loss (dB)
6.4 to 13 13 to 384	6 8

6.2.1.3 Specifications at the input ports

The digital signal presented at the input port shall be as defined above but modified by the characteristics of the interconnecting pairs. The attenuation of these pairs at a frequency of 128 kHz should be in the range 0 to 3 dB. This attenuation should take into account any losses incurred by the presence of a digital distribution frame between the equipment.

For the jitter to be tolerated at the input port, refer to clause 7.1.1 of [ITU-T G.823].

The return loss at the input ports should have the minimum values given in Table 6-3:

Table 6-3 – Digital 64 kbit/s codirectional interface input port minimum return loss

Frequency range (kHz)	Return loss (dB)
4 to 13 13 to 256 256 to 384	12 18 14

To provide nominal immunity against interference, input ports are required to meet the following requirements:

A nominal aggregate signal, encoded as a 64 kbit/s codirectional signal and having a pulse shape as defined in the pulse mask, shall have added to it an interfering signal with the same pulse shape as the wanted signal. The interfering signal should have a bit rate within the limits specified in this Recommendation, but should not be synchronous with the wanted signal. The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance 120 ohms to give a signal-to-interference ratio of 20 dB. The binary content of the interfering signal should comply with [ITU-T O.152] ($2^{11} – 1$ bit period). No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the input port.

6.2.1.4 Grounding of screen

If the symmetrical pair is screened, the screen shall be connected to the bonding network both at the input port and output port.

NOTE 1 – The cable routing is important if leaving the system block. Consult [ITU-T K.27] for guidance.

NOTE 2 – The use of isolation to the bonding network is for further study.

6.2.2 Electrical characteristics of the 64 kbit/s centralized clock interface

6.2.2.1 General characteristics

Nominal bit rate: 64 kbit/s. The tolerance is determined by the network clock stability (see [ITU-T G.811]).

For each direction of transmission, there should be one symmetrical pair carrying the data signal. In addition, there should be symmetrical pairs carrying the composite timing signal (64 kHz and 8 kHz) from the central clock source to the office terminal equipment. The use of transformers is recommended.

Overvoltage protection requirements: refer to [ITU-T K.20].

Code conversion rules:

The data signals are coded in AMI code with a 100% duty ratio. The composite timing signals convey the 64 kHz bit-timing information using AMI code with a 50% to 70% duty ratio and the 8 kHz octet-phase information by introducing violations of the code rule. The structure of the signals and their nominal phase relationships are shown in Figure 6-6.

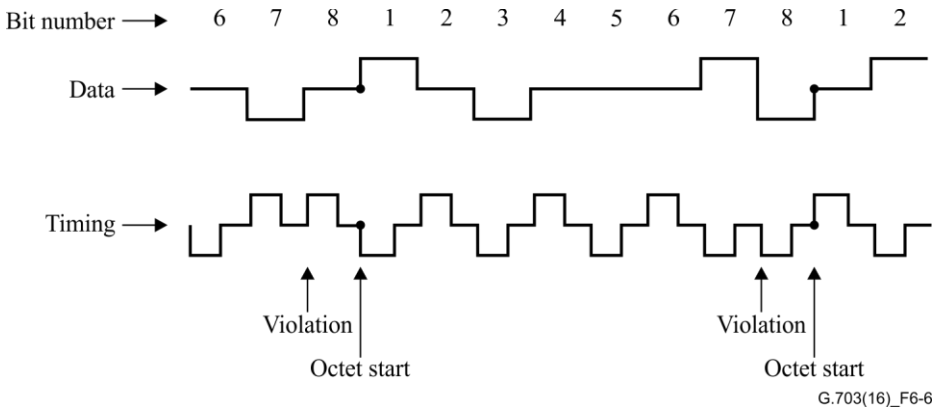


Figure 6-6 – Signal structures of the 64-kbit/s central clock interface at office terminal output ports

The data stream at the output ports should be timed by the leading edge of the timing pulse and the detection instant at the input ports should be timed by the trailing edge of each timing pulse.

6.2.2.2 Characteristics at the output ports

See Table 6-4.

Table 6-4 – Digital 64 kbit/s centralized clock interface

Parameters	Data	Timing
Pulse shape	Nominally rectangular, with rise and fall times less than 1 μs	Nominally rectangular, with rise and fall times less than 1 μs
Nominal test load impedance	110 ohms resistive	110 ohms resistive
Peak voltage of a "mark" (pulse) (Note 1)	a) 1.0 ± 0.1 V b) 3.4 ± 0.5 V	a) 1.0 ± 0.1 V b) 3.0 ± 0.5 V
Peak value of a "space" (no pulse) (Note 1)	a) 0 ± 0.1 V b) 0 ± 0.5 V	a) 0 ± 0.1 V b) 0 ± 0.5 V
Nominal pulse width (Note 1)	a) 15.6 μs b) 15.6 μs	a) 7.8 μs b) 9.8 to 10.9 μs
Maximum peak-to-peak jitter at the output port (Note 2)	Refer to clause 5.1 of [ITU-T G.823]	
NOTE 1 – The choice between the set of parameters a) and b) allows for different office noise environments and different maximum cable lengths between the three involved office equipment. NOTE 2 – For the time being, these values are valid only for equipment of the 2 Mbit/s hierarchy.		

6.2.2.3 Characteristics at the input ports

The digital signals presented at the input ports should be as defined above but modified by the characteristics of the interconnecting pairs. The varying parameters in Table 6-4 will allow typical maximum interconnecting distances of 350 to 450 m.

6.2.2.4 Cable characteristics

The transmission characteristics of the cable to be used are subject to further study.

6.2.3 Electrical characteristics of 64 kbit/s contradirectional interface

6.2.3.1 General characteristics

Nominal bit rate: 64 kbit/s.

Bit rate accuracy: ±100 ppm (±6.4 bit/s) or better.

For each direction of transmission there should be two symmetrical pairs of wires, one pair carrying the data signal and the other carrying a composite timing signal (64 kHz and 8 kHz). The use of transformers is recommended.

NOTE – If there is a national requirement to provide a separate alarm signal across the interface, this can be done by cutting the 8 kHz timing signal for the transmission direction concerned, i.e., by inhibiting the code violations introduced in the corresponding composite timing signal (see below).

Code conversion rules:

The data signals are coded in AMI code with a 100% duty ratio. The composite timing signals convey the 64 kHz bit-timing information using AMI code with a 50% duty ratio and the 8 kHz octet-phase information by introducing violations of the code rule. The structures of the signals and their phase relationships at data output ports are shown in Figure 6-7.

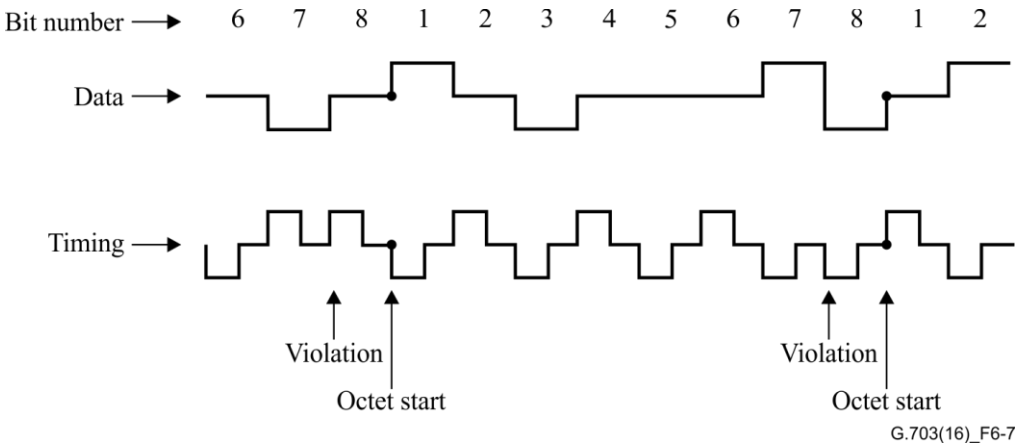


Figure 6-7 – Signal structures of the 64-kbit/s contradirectional interface at data output ports

The data pulses received from the service (e.g., data or signalling) side of the interface will be somewhat delayed in relation to the corresponding timing pulses. The detection instant for a received data pulse on the line side (e.g., PCM) of the interface should therefore be at the leading edge of the next timing pulse.

Overvoltage protection requirements: refer to [ITU-T K.20].

6.2.3.2 Specifications at the output ports

See Table 6-5.

Table 6-5 – Digital 64 kbit/s contradirectional interface

Parameters	Data	Timing
Pulse shape (nominally rectangular)	All pulses of a valid signal must conform to the mask in Figure 6-8 irrespective of the polarity	All pulses of a valid signal must conform to the mask in Figure 6-9 irrespective of the polarity
Pairs in each direction of transmission	One symmetric pair	One symmetric pair
Test load impedance	120 ohms resistive	120 ohms resistive
Nominal peak voltage of a "mark" (pulse)	1.0 V	1.0 V
Peak voltage of a "space" (no pulse)	0 V ± 0.1 V	0 V ± 0.1 V
Nominal pulse width	15.6 µs	7.8 µs
Ratio of the amplitudes of positive and negative pulses at the centre of the pulse interval	0.95 to 1.05	0.95 to 1.05
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05	0.95 to 1.05
Maximum peak-to-peak jitter at the output port (Note)	Refer to clause 5.1 of [ITU-T G.823]	
NOTE – For the time being these values are valid only for equipment of the 2 Mbit/s hierarchy.		

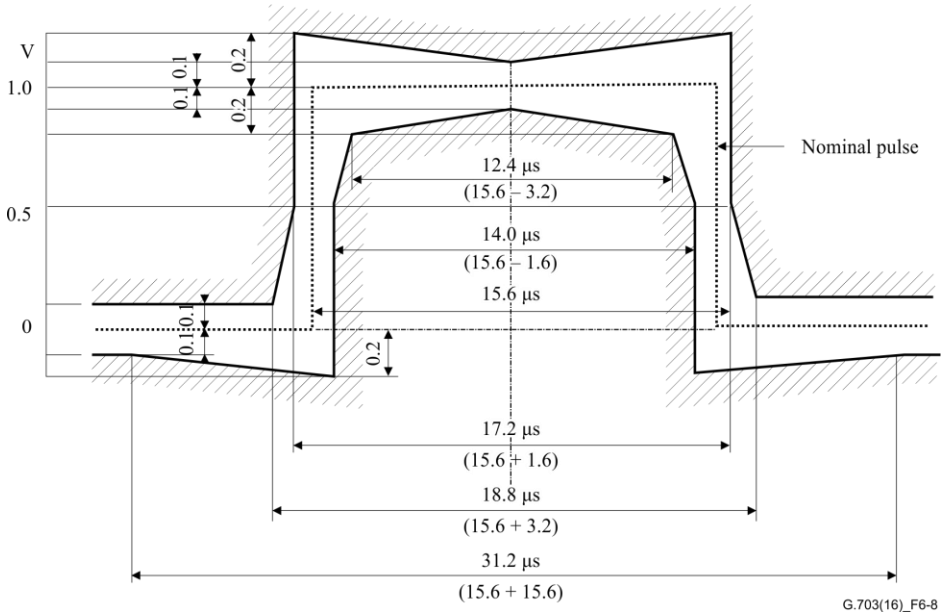


Figure 6-8 – Mask of the data pulse of the 64-kbit/s contradirectional interface

NOTE 1 – When one pulse is immediately followed by another pulse of the opposite polarity, the time limits at the zero-crossing between the pulses should be ±0.8 µs.

NOTE 2 – The time instants at which a transition from one state to another in the data signal may occur are determined by the timing signal. On the service (e.g., data or signalling) side of the interface, it is essential that these transitions are not initiated in advance of the timing instants given by the received timing signal.

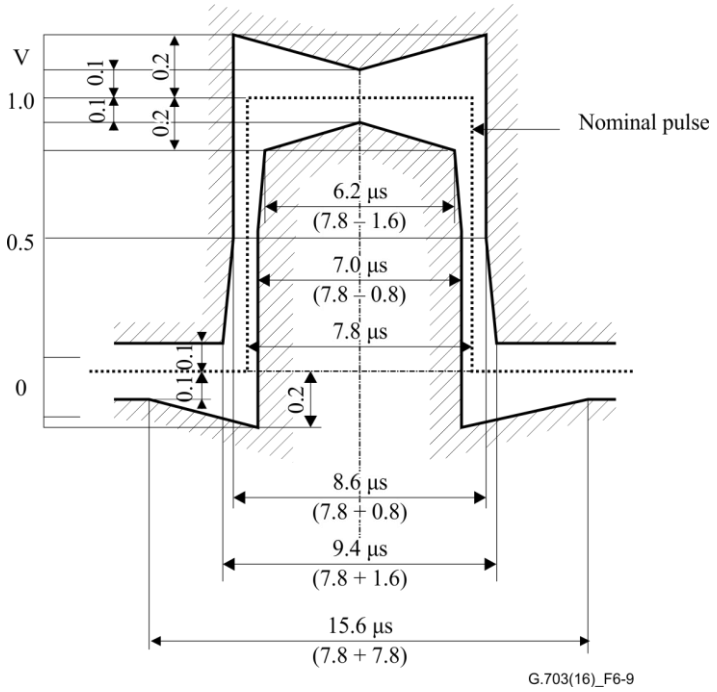


Figure 6-9 – Mask of the timing pulse of the 64-kbit/s contradirectional interface

6.2.3.3 Specifications at the input ports

The digital signals presented at the input ports should be as defined above but modified by the characteristics of the interconnecting pairs. The attenuation of these pairs at a frequency of 32 kHz should be in the range 0 to 3 dB. This attenuation should take into account any losses incurred by the presence of a digital distribution frame between the equipment.

The return loss at the input ports should have the minimum values given in Table 6-5:

Table 6-5 – Digital 64 kbit/s contradirectional interface input port minimum return loss

Frequency range (kHz)		Return loss (dB)
Data signal	Composite timing signal	
1.6 to 3.2	3.2 to 6.4	12
3.2 to 64	6.4 to 128	18
64 to 96	128 to 192	14

To provide nominal immunity against interference, input ports are required to meet the following requirement:

A nominal aggregate signal, encoded as a 64 kbit/s contradirectional signal and having a pulse shape as defined in the pulse mask, shall have added to it an interfering signal with the same pulse shape as the wanted signal. The interfering signal should have a bit rate within the limits specified in this Recommendation, but should not be synchronous with the wanted signal. The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance 120 ohms to give a signal-to-interference ratio of 20 dB. The binary content of the interfering signal should comply with [ITU-TO.152] (2^{11} – 1 bit period). No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the input port.

NOTE – The return loss specification applies for both the data signal and the composite timing signal input ports.

6.2.3.4 Grounding of screen

If the symmetrical pairs are screened, the screens shall be connected to the bonding network both at the input port and the output port.

NOTE 1 – The cable routing is important if leaving the system block. Consult [ITU-T K.27] for guidance.

NOTE 2 – The use of isolation to the bonding network is for further study.

7 Interface at 1544 kbit/s (E11)

7.1 General characteristics

The digital interface signal has a nominal bit rate of 1544 kbit/s.

The 1544 kbit/s interface specification is defined in Table 7-1. All signals appearing at the 1544 kbit/s interface shall satisfy each requirement listed.

Table 7-1 –Digital interface at 1544 kbit/s

Parameter	Specification
Nominal bit rate	1544 kbit/s
Line rate accuracy	In a self-timed, free running mode, the bit rate accuracy shall be ±50 bits/s (±32 ppm) or better.
Line code	Either 1) AMI with no more than 15 consecutive zeros, and at least N ones in each and every time window of 8(N + 1) digit time slots (where N can range from 1 to 23), or 2) B8ZS (Note 1).
Frame structure	No frame structure is required for 1544 kbit/s transmission or higher level multiplexing to higher level DSN signals.
Medium	One balanced twisted pair shall be used for each direction of transmission.
Test load impedance	A resistive test load of 100 ohms ±5% shall be used at the interface for the evaluation of pulse shape and the electrical parameters specified below.
Pulse amplitude	The amplitude (Note 2) of an isolated pulse shall be between 2.4 V and 3.6 V.
Pulse shape	The shape of every pulse that approximates an isolated pulse (is preceded by four zeros and followed by one or more zeros) shall conform to the mask in Figure 7-1. See clause 7.2 for allowable procedures to be followed in checking conformance.
Power level	For an all-one signal, the power in a 3 kHz ± 1 kHz band centered at 772 kHz shall be between 12.6 dBm and 17.9 dBm. The power in a 3 kHz ± 1 kHz band centered at 1544 kHz shall be at least 29 dB below that at 772 kHz.
Pulse imbalance	In any window of seventeen consecutive bits, the maximum variation in pulse amplitudes shall be less than 200 mV, and the maximum variation in pulse widths (half amplitude) shall be less than 20 ns.
DC power	There shall be no DC power applied at the interface.
Verification access	Access to the signal at the interface shall be provided for verification of these signal specifications.
NOTE 1 – B8ZS is one method of providing bit sequence independence. Bit sequence independence in turn allows unconstrained clear channel capability. Zero Byte Time Slot Interchange (ZBTSI) is another method of providing clear channel transmission. NOTE 2 – While both voltage and power requirements are given to assist in qualification of signals at the interface, the values are not equivalent. Voltage specifications are given for isolated pulses, while power levels are specified for all-ones signal.	

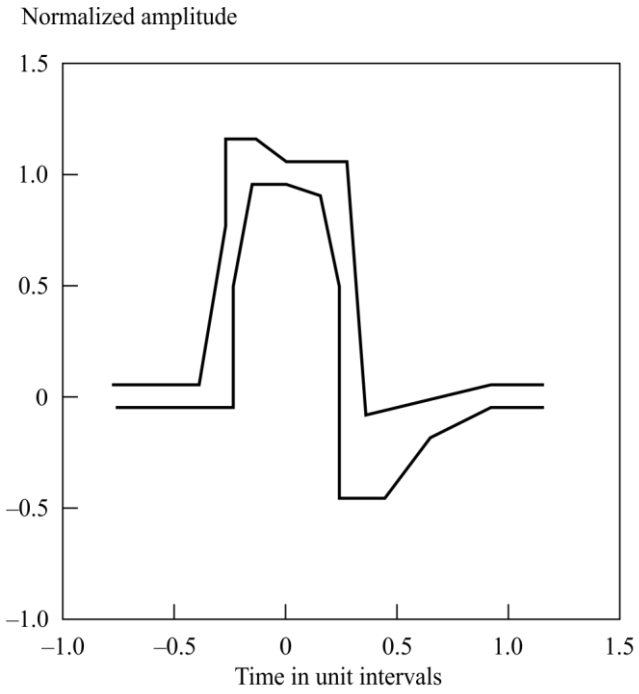
Jitter requirements:

– for the maximum peak-to-peak jitter at the output port, refer to clause 5.1 of [ITU-T G.824];

– for the jitter to be tolerated at the input port, refer to clause 7.2.1 of [ITU-T G.824].

Overvoltage protection requirements: refer to [ITU-T K.20].

An isolated pulse at the 1544 kbit/s interface shall fit within the mask shown in Figure 7-1. The corner points for this mask are shown below the figure. In this figure, the y axis shows normalized pulse amplitude. The x axis is time measured in unit intervals. For 1544 kbit/s, the unit interval is 648 ns.



Minimum curve		Maximum curve	
Time	**Normalized amplitude**	**Time**	**Normalized amplitude**
– 0.77	– 0.05	– 0.77	0.05
– 0.23	– 0.05	– 0.39	0.05
– 0.23	0.5	– 0.27	0.8
– 0.15	0.95	– 0.27	1.15
0.0	0.95	– 0.12	1.15
0.15	0.9	0.0	1.05
0.23	0.5	0.27	1.05
0.23	– 0.45	0.35	– 0.07
0.46	– 0.45	0.93	0.05
0.66	– 0.2	1.16	0.05
0.93	– 0.05		
1.16	– 0.05		

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Figure 7-1 – 1544 kbit/s interface isolated pulse mask and corner points

Some 1544 kbit/s interface equipment embedded in the network may have been designed using a different pulse mask than that in this Recommendation. Appendix I describes the earlier specification to provide information to designers of receiving equipment on the possible range of 1544 kbit/s signals in the network.

To accommodate signals generated by equipment predating this Recommendation, the (1544 kbit/s) receivers should be capable of operation with a signal having a transmission rate of deviation of ±200 bit/s (±130 ppm) (see Appendix I for pulse characteristics of older equipment).

7.2 Pulse specification

For alternate mark inversion (AMI) coding, a pulse mask describing an isolated pulse appearing at the interface is used. In most cases, an ideal isolated pulse can only be approximated due to line coding constraints.

Pulse masks are shown in normalized form, with the nominal pulse amplitude shown as 1.0. In judging conformance of an isolated pulse to the mask, it is only permissible to:

a) position the mask horizontally as needed to encompass the pulse; and

b) uniformly scale the amplitude of the isolated pulse to fit the mask.

The baseline of the signal shall coincide with the zero point of the baseline of the mask. (The determination of the signal baseline is described in [IEC 60469-2]). Judging the conformance of negative-going pulses shall be performed after determining the conformance of positive-going pulses in order to maintain the signal baseline reference.

When viewing inverted negative-going pulses for 1544 kbit/s, only the horizontal positioning of the mask to encompass the pulse is permitted. Note that pulse streams with any significant DC component will not meet the requirements of this clause.

7.3 Eye diagrams

For signals not amenable to the use of pulse masks, another means of specifying the quality of pulses at the interface is an eye diagram, which is formed by superimposing the waveforms of all possible pulse sequences, including the effects of intersymbol interference. Eye diagrams are presented in normalized form with the peak pulse amplitudes normalized to 1.0 on the vertical scale and the time scale shown in terms of the unit interval. In judging the shape of an eye diagram, it is permissible to:

a) position the mask horizontally as needed to encompass the eye diagram; and

b) uniformly scale the amplitude of the mask as needed to encompass the eye diagram.

The baseline of the mask shall coincide with the signal baseline. The determination of signal baseline is described in [IEC 60469-2].

8 Interface at 6312 kbit/s (E21)

Interconnection of 6312 kbit/s signals for transmission purposes is accomplished at a digital distribution frame.

Nominal bit rate: 6312 kbit/s.

Bit rate accuracy: ±30 ppm (189.4 bit/s) or better.

A pseudo-ternary code shall be used as indicated in Table 8-1.

The shape for an isolated pulse measured at the distribution frame shall fall within the mask either of Figure 8-1 or of Figure 8-2 and meet the other requirements of Table 8-1.

Table 8-1 – Digital interface at 6312 kbit/s (Note 1)

Parameter	Specification	
Bit rate	6312 kbit/s	
Pair(s) in each direction of transmission	One symmetric pair	One coaxial pair
Code	B6ZS (Note 2)	B8ZS (Note 2)
Test load impedance	110 ohms ± 5% resistive	75 ohms ± 5% resistive
Nominal pulse shape (Note 1)	Rectangular, shaped by cable loss (see Figure 11)	Rectangular (see Figure 12)
Signal level	For an all 1s pattern transmitted, the power measured in a 3 kHz bandwidth should be as follows:	
	3156 kHz: 0.2 to 7.3 dBm 6312 kHz: −20 dBm or less	3156 kHz: 6.2 to 13.3 dBm 6312 kHz: −14 dBm or less
NOTE 1 – The pulse mask for 2nd order digital interface is shown in Figures 8-1 and 8-2. NOTE 2 – See Annex A.		

The voltage within a time slot containing a zero (space) shall be no greater than either the value produced in that time slot by other pulses (marks) within the mask of Figure 11, or ±0.1 of the peak pulse (mark) amplitude, whichever is greater in magnitude.

Jitter requirements:

– For the maximum peak-to-peak jitter at the output port, refer to clause 5.1 of [ITU-T G.824];

– For the jitter to be tolerated at the input port, refer to clause 7.2.2 of [ITU-T G.824].

Overvoltage protection requirements: refer to [ITU-T K.20].

	T	Value of curve
Lower curve	$T \le 0.41$	0
	$-0.41 \le T \le 0.24$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.205}\right)\right]$
	$0.24 \le T$	$0.331e^{-1.9(T-0.3)}$
Upper curve	$T \le 0.72$	0
	$-0.72 \le T \le 0.2$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.36}\right)\right]$
	$0.2 \le T$	$0.1 + 0.721e^{-2.13(T-0.2)}$

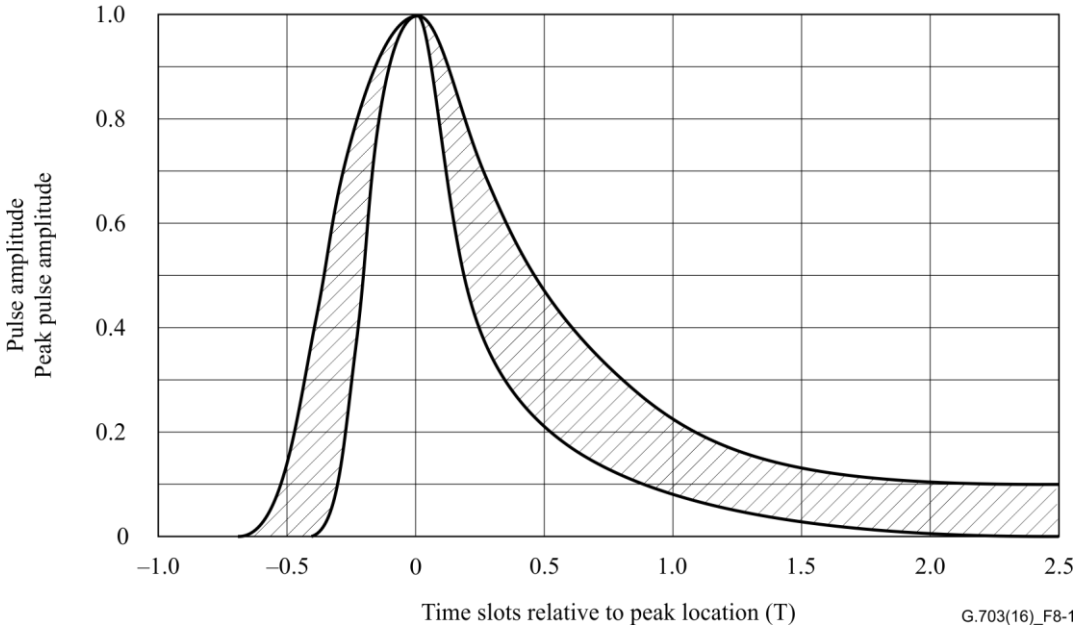


Figure 8-1 – Pulse mask for the symmetric pair interface at 6312 kbit/s

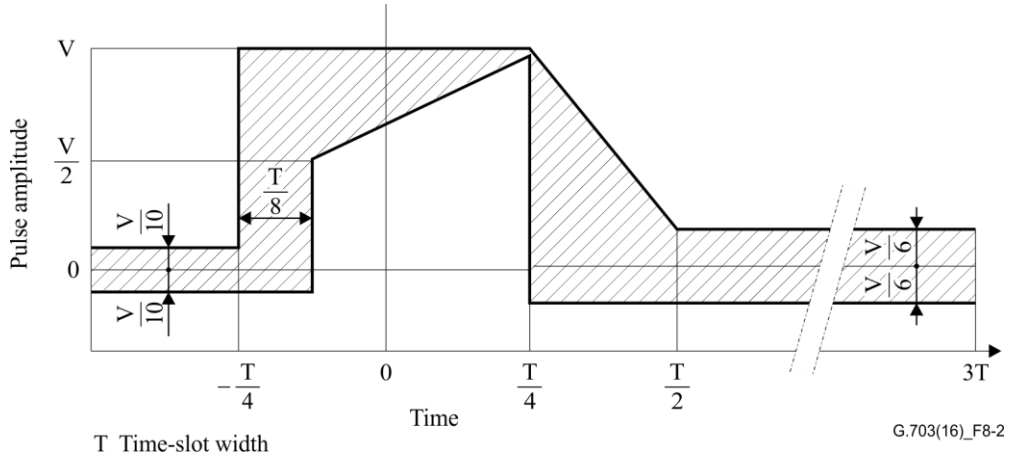


Figure 8-2 – Pulse mask for the coaxial pair interface at 6312 kbit/s

9 Interface at 32 064 kbit/s

Interconnection of 32 064 kbit/s signals for transmission purposes is accomplished at a digital distribution frame.

Nominal bit rate: 32 064 kbit/s.

Bit rate accuracy: ±10 ppm (±320.6 bit/s).

One coaxial pair shall be used for each direction of transmission.

The test load impedance shall be 75 ohms ± 5% resistive and the test method shall be direct.

A scrambled AMI code shall be used.

The shape for an isolated pulse measured at the point where the signal arrives at the distribution frame shall fall within the mask in Figure 9-1.

	T	Value of curve
Lower curve	$-0.36 \le T \le -0.30$	$5.76T + 2.07$
	$-0.30 \le T < 0$	$0.5\left[1+\sin\frac{\pi}{2}\left(1+\frac{T}{0.25}\right)\right]$
	$0 \le T < 0.22$	$0.5\left[1+\sin\frac{\pi}{2}\left(1+\frac{T}{0.16}\right)\right]$
	$0.22 \le T$	$0.11e^{-3.42(T-0.3)}$
Upper curve	$-0.65 \le T < 0$	$1.05\left[1-e^{-4.6(T+0.65)}\right]$
	$0 \le T < 0.25$	$0.5\left[1+\sin\frac{\pi}{2}\left(1+\frac{T}{0.28}\right)\right]$
	$0.25 \le T$	$0.11+0.407e^{-2.1(T-0.29)}$

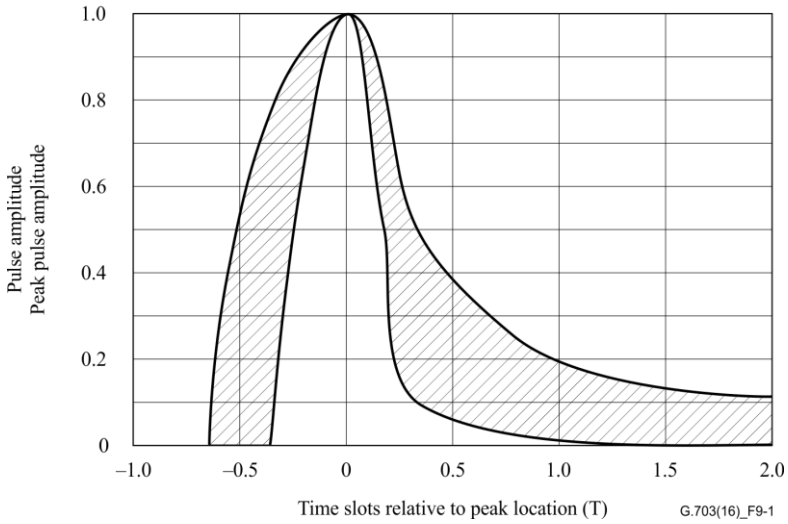


Figure 9-1 – Pulse mask for the coaxial pair interface at 32 064 kbit/s

The voltage within a time slot containing a zero (space) shall be no greater than either the value produced in that time slot by other pulses (marks) within the mask of Figure 9-1 or ±0.1 of the peak pulse (mark) amplitude, whichever is greater in magnitude.

For an all 1s pattern transmitted, the power measured in a 3 kHz bandwidth at the point where the signal arrives at the distribution frame shall be as follows:

– 16 032 kHz: + 5 dBm to + 12 dBm;

– 32 064 kHz: at least 20 dB below the power at 16 032 kHz.

The connectors and coaxial cable pairs in the distribution frame shall be 75 ohms ± 5%.

Jitter requirements:

– For the maximum peak-to-peak jitter at the output port, refer to clause 5.1 of [ITU-T G.824];

– For the jitter to be tolerated at the input port, refer to clause 7.2.3 of [ITU-T G.824].

Overvoltage protection requirements: refer to [ITU-T K.20].

10 Interface at 44 736 kbit/s (E32)

44 736 kbit/s interface specification is defined in Table 10-1.

Table 10-1 – Digital interface at 44 736 kbit/s

Parameter	Specification
Nominal bit rate	44 736 kbit/s
Bit rate accuracy	In a self-timed, free-running mode, the bit rate accuracy shall be ±895 bits/s (±20 ppm) or better.
Line code	B3ZS (bipolar with three-zero substitutions)
Frame structure	The signal shall have the frame structure defined in [ITU-T G.752] to ensure transmission through all types of 44 736 kbit/s transport equipment. The frame structure is not required for multiplexing to higher level DSN signals.
Medium	One unbalanced coaxial line shall be used for each direction of transmission.
Test load impedance	A resistive test load of 75 ohms ± 5% shall be used at the interface for the evaluation of pulse shape and the electrical parameters specified below.
Pulse amplitude	The amplitude (Note 1) of an isolated pulse shall be between 0.36 V and 0.85 V peak.
Pulse shape	The shape of every pulse that approximates an isolated pulse (is preceded by two zeros and followed by one or more zeros) shall conform to the mask in Figure 10-1. See clause 7.2 for allowable procedures to be followed in checking conformance. This mask includes an allowance of ±3% of the peak pulse amplitude at any point on the mask relative to the pulse mask in the earlier version. Equations defining the various line segments making up the mask are listed below the figure.
Power level	A wideband power measurement of an AIS signal (as defined in [ITU-T G.704]) using a power level sensor with a working frequency range of 200 MHz shall be between −4.7dBm and +3.6 dBm, including the effects of a range of connecting cable lengths between 68.6 meters (225 feet) and 137.2 meters (450 feet). A low-pass filter having a flat passband and cutoff frequency of 200 MHz shall be used. The rolloff characteristics of this filter are not important; or an alternate power level specification of the power of an all-ones signal (Note 2) is useful for some equipment qualifications. It requires that the power in a 3 kHz ± 1 kHz band centered at 22 368 kHz be between −1.8 dBm and +5.7 dBm. It further requires that the power in a 3 kHz ± 1 kHz band centered at 44 736 kHz be at least 20 dB below that at 22 368 kHz.
Pulse imbalance	1) The ratio of amplitudes of positive and negative isolated pulses shall be between 0.90 and 1.10. 2) Positive and negative isolated pulses shall both conform to the mask of Figure 10-1.
DC power	There shall be no DC power applied at the interface.
Verification access	Access to the signal at the interface shall be provided for verification of these signal specifications.
NOTE 1 – While both voltage and power requirements are given to assist in qualification of signals at the interface, the values are not equivalent. Voltage specifications are given for isolated pulses, while power levels are specified for an AIS signal, or alternatively an all-ones signal. NOTE 2 – The all-ones signal is not realizable within the frame structure specified in [ITU-T G.752], and is not encountered in North American telecommunication networks.	

All signals appearing at the 44 736 kbit/s interface shall satisfy each requirement listed.

An isolated pulse (see pulse shape in Table 10-1) at the 44 736 kbit/s interface shall fit within the mask shown in Figure 14. Equations defining the various line segments making up the mask are listed below the figure. In this figure, the y axis shows normalized pulse amplitude. The x axis is time measured in unit intervals. For 44 736 kbit/s, the unit interval is 22.4 ns.

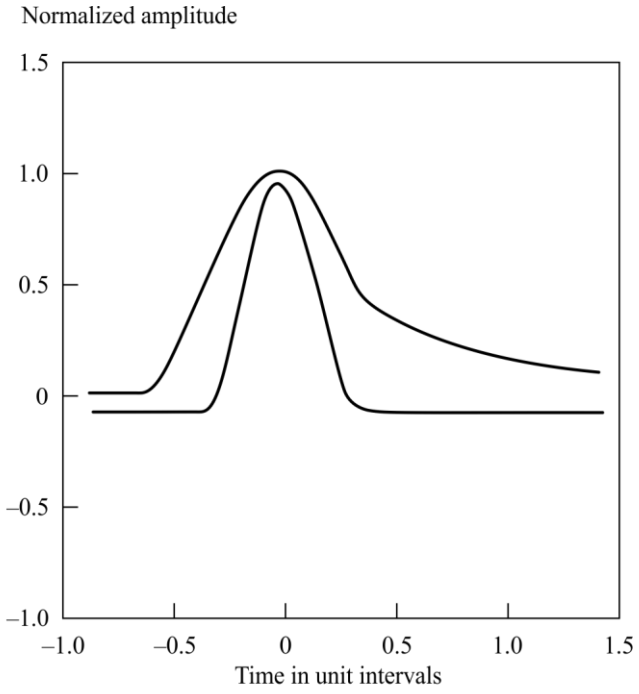
To assure proper operation of transmission facilities and higher order multiplex equipment, all 44 736 kbit/s sources shall use the frame structured defined in [ITU-T G.752].

Jitter requirements:

– for the maximum peak-to-peak jitter at the output port, refer to clause 5.1 of [ITU-T G.824];

– for the jitter to be tolerated at the input port, refer to clause 7.2.4 of [ITU-T G.824].

Overvoltage protection requirements: refer to [ITU-T K.20].



Time axis range (Unit Intervals)	Normalized amplitude equation
Upper curve	
$-0.85 \le T \le -0.68$	0.03
$-0.68 \le T \le 0.36$	$0.5\left\{1+\sin\left[\frac{\pi}{2}\left(1+\frac{T}{0.34}\right)\right]\right\}+0.03$
$0.36 \le T \le 1.4$	$0.08+0.407e^{-1.84(T-0.36)}$
Lower curve	
$-0.85 \le T \le -0.36$	–0.03
$-0.36 \le T \le 0.36$	$0.5\left\{1+\sin\left[\frac{\pi}{2}\left(1+\frac{T}{0.18}\right)\right]\right\}-0.03$
$0.36 \le T \le 1.4$	–0.03

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Figure 10-1 – 44 736 kbit/s interface isolated pulse mask and equations

11 Interface at 2048 kbit/s (E12)

11.1 General characteristics

Nominal bit rate: 2048 kbit/s.

Bit rate accuracy: ±50 ppm (±102.4 bit/s).

Code: High density bipolar of order 3 (HDB3) (a description of this code can be found in Annex A).

Overvoltage protection requirements: refer to [ITU-T K.20].

11.2 Specifications at the output ports

See Table 11-1. See also Note 6 of clause 1.

Table 11-1 – Digital interface at 2048 kbit/s

Parameter	Specification	
Pulse shape (nominally rectangular)	All marks of a valid signal must conform with the mask (see Figure 11-1) irrespective of the sign. The value V corresponds to the nominal peak value.	
Pair(s) in each direction	One coaxial pair (see clause 11.4)	One symmetrical pair (see clause 11.4)
Test load impedance	75 ohms resistive	120 ohms resistive
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 ± 0.237 V	0 ± 0.3 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the centre of the pulse interval	0.95 to 1.05	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05	
Maximum peak-to-peak jitter at an output port	Refer to clause 5.1 of [ITU-T G.823]	

The return loss at the output port should have the minimum values given in Table 11-2:

Table 11-2 – Digital interface at 2048 kbit/s output port minimum return loss

Frequency range (kHz)	Return loss (dB)
51 to 102 102 to 3072	6 8

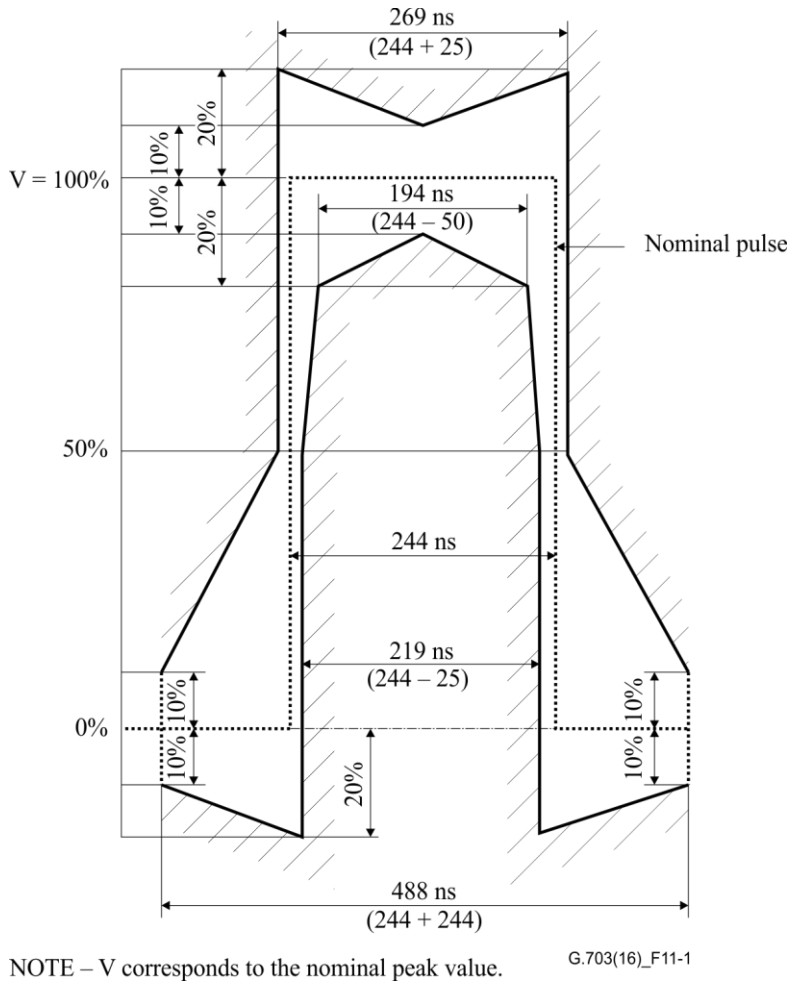


Figure 11-1 – Mask of the pulse at the 2048 kbit/s interface

11.3 Specifications at the input ports

The digital signal presented at the input port shall be as defined above but modified by the characteristic of the interconnecting pair. The attenuation of this pair shall be assumed to follow a $\sqrt{f}$ law and the loss at a frequency of 1024 kHz shall be in the range 0 to 6 dB. This attenuation should take into account any losses incurred by the presence of a digital distribution frame between the equipment.

For the jitter to be tolerated at the input port, refer to clause 7.1.2 of [ITU-T G.823].

The return loss at the input port should have the provisional minimum values given in Table 11-3:

Table 11-3 – Digital interface at 2048 kbit/s input port minimum return loss

Frequency range (kHz)	Return loss (dB)
51 to 102	12
102 to 2048	18
2048 to 3072	14

To ensure adequate immunity against signal reflections that can arise at the interface due to impedance irregularities at digital distribution frames and at digital output ports, input ports should meet the following requirement:

A nominal aggregate signal, encoded into HDB3 and having a pulse shape as defined in the pulse mask, shall have added to it an interfering signal with the same pulse shape as the wanted signal. The interfering signal should have a bit rate within the limits specified in this Recommendation, but should not be synchronous with the wanted signal. The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance 75 ohms (in the case of coaxial-pair interface) or 120 Ohms (in the case of symmetrical-pair interface), to give a signal-to-interference ratio of 18 dB. The binary content of the interfering signal should comply with [ITU-T O.151] ($2^{15} – 1$ bit period). No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the input port.

NOTE – A receiver implementation providing an adaptive rather than a fixed threshold is considered to be more robust against reflections and should therefore be preferred.

11.4 Grounding of outer conductor or screen

The outer conductor of the coaxial pair or the screen of the symmetrical pair shall be connected to the bonding network both at the input port and the output port.

NOTE 1 – The cable routing is important if leaving the system block. Consult [ITU-T K.27] for guidance.

NOTE 2 – The direct connection of the outer conductors of coaxial cables to the bonding network at the transmit and receive interfaces may, because of differences in earth potential at each end of the cable, result in unwanted current flowing in the outer conductor, through connectors and through the receiver input circuitry. This may result in errors or even permanent damage. To prevent this problem, DC isolation may be introduced between the outer conductor and bonding network at the receive interface. The method of DC isolation must not compromise the EMC compliance of the equipment and the overall installation.

NOTE 3 – The use of isolation to the bonding network is for further study.

12 Interface at 8448 kbit/s (E22)

12.1 General characteristics

Nominal bit rate: 8448 kbit/s.

Bit rate accuracy: ±30 ppm (±253.4 bit/s).

Code: High density bipolar of order 3 HDB3 (a description of this code can be found in Annex A).

Overvoltage protection requirements: refer to [ITU-T K.20].

12.2 Specification at the output ports

See Table 12-1. See also Note 6 of clause 1.

Table 12-1 – Digital interface at 8448 kbit/s

Parameter	Specification
Pulse shape (nominally rectangular)	All marks of a valid signal must conform with the mask (Figure 12-1) irrespective of the sign.
Pair(s) in each direction	One coaxial pair (see clause12.4)
Test load impedance	75 ohms resistive
Nominal peak voltage of a mark (pulse)	2.37 V
Peak voltage of a space (no pulse)	0 V ± 0.237 V

Table 12-1 – Digital interface at 8448 kbit/s

Parameter	Specification
Nominal pulse width	59 ns
Ratio of the amplitudes of positive and negative pulses at the centre of the pulse interval	0.95 to 1.05
Ratio of widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05
Maximum peak-to-peak jitter at an output port	Refer to clause 5.1 of [ITU-T G.823]

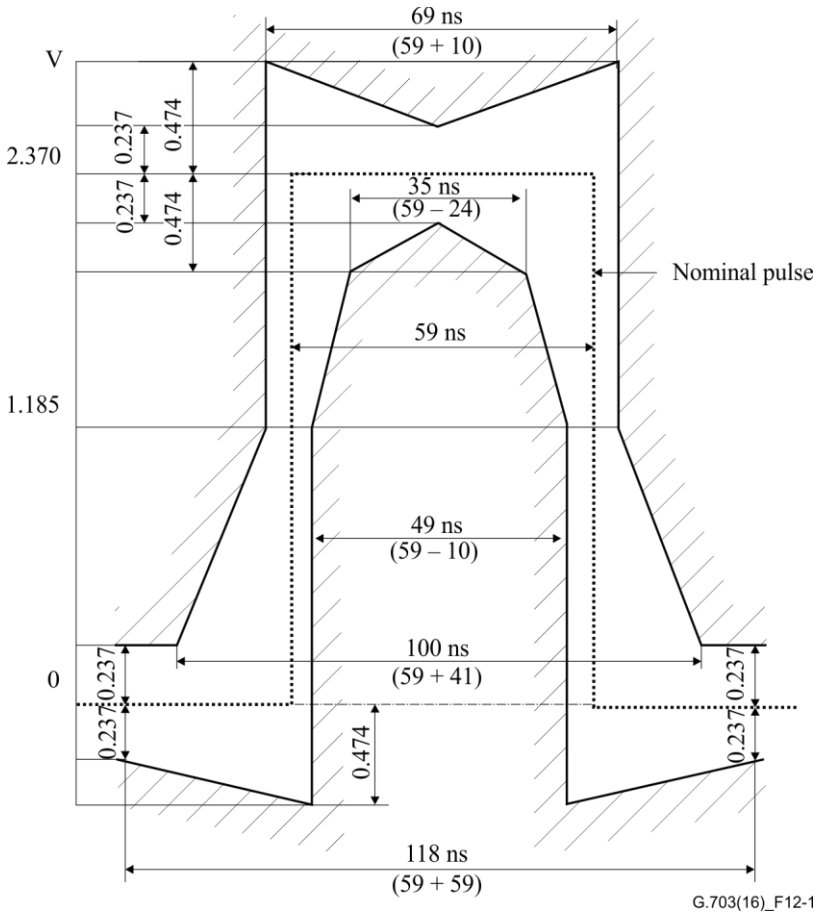


Figure 12-1 – Pulse mask at the 8448 kbit/s interface

The return loss at the output port should have the minimum values given in Table 12-2:

Table 12-2 – Digital interface at 8448 kbit/s output port minimum return loss

Frequency range (kHz)	Return loss (dB)
211 to 422 422 to 12 672	6 8

12.3 Specifications at the input ports

The digital signal presented at the input port shall be as defined above but modified by the characteristics of the interconnecting pairs. The attenuation of this pair shall be assumed to follow a $\sqrt{f}$ law and the loss at a frequency of 4224 kHz shall be in the range 0 to 6 dB. This attenuation should take into account any losses incurred by the presence of a digital distribution frame between the equipment.

For the jitter to be tolerated at the input port, refer to clause 7.1.3 of [ITU-T G.823].

The return loss at the input port should have the provisional minimum values given in Table 12-3:

Table 12-3 – Digital interface at 8448 kbit/s input port minimum return loss

Frequency range (kHz)	Return loss (dB)
211 to 422	12
422 to 8448	18
8448 to 12 672	14

To ensure adequate immunity against signal reflections that can arise at the interface due to impedance irregularities at digital distribution frames and at digital output ports, input ports should meet the following requirement:

A nominal aggregate signal, encoded into HDB3 and having a pulse shape as defined in the pulse mask shall have added to it an interfering signal with the same pulse shape as the wanted signal. The interfering signal should have a bit rate within the limits specified in this Recommendation, but should not be synchronous with the wanted signal. The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance 75 ohms to give a signal-to-interference ratio of 20 dB. The binary content of the interfering signal should comply with [ITU-T O.151] ($2^{15} – 1$ bit period). No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the input port.

12.4 Grounding of outer conductor

The outer conductor of the coaxial pair shall be connected to the bonding network at the input port and the output port.

NOTE 1 – The cable routing is important if leaving the system block. Consult [ITU-T K.27] for guidance.

NOTE 2 – The use of isolation to the bonding network is for further study.

13 Interface at 34 368 kbit/s (E31)

13.1 General characteristics

Nominal bit rate: 34 368 kbit/s.

Bit rate accuracy: ±20 ppm (±688 bit/s).

Code: HDB3 (a description of this code can be found in Annex A).

Overvoltage protection requirements: refer to [ITU-T K.20].

13.2 Specification at the output ports

See Table 13-1. See also Note 6 of clause 1.

Table 13-1 – Digital interface at 34 368 kbit/s

Parameter	Specification
Pulse shape (nominally rectangular)	All marks of a valid signal must conform with the mask (see Figure 13-1), irrespective of the sign.
Pair(s) in each direction	One coaxial pair (see clause 13.4)
Test load impedance	75 ohms resistive
Nominal peak voltage of a mark (pulse)	1.0 V
Peak voltage of a space (no pulse)	0 V ± 0.1 V
Nominal pulse width	14.55 ns
Ratio of the amplitudes of positive and negative pulses at the center of a pulse interval	0.95 to 1.05
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05
Maximum peak-to-peak jitter at an output port	Refer to clause 5.1 of [ITU-T G.823]

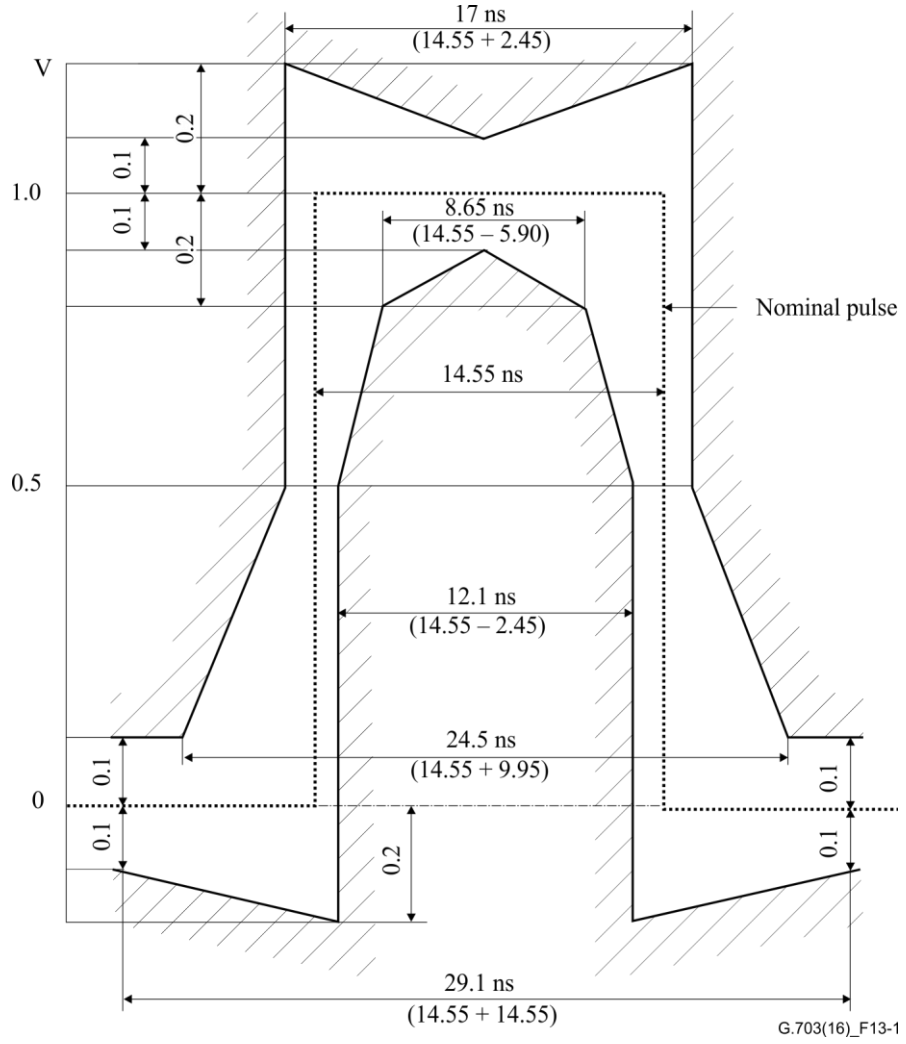


Figure 13-1 – Pulse mask at the 34 368 kbit/s interface

The return loss at the output port should have the minimum values shown in Table 13-2:

Table 13-2 – Digital interface at 34 368 kbit/s output port minimum return loss

Frequency range (kHz)	Return loss (dB)
860 to 1720 1720 to 51 550	6 8

13.3 Specifications at the input ports

The digital signal presented at the input port shall be as defined above but modified by the characteristics of the interconnecting pair. The attenuation of this cable shall be assumed to follow approximately a $\sqrt{f}$ law (i.e., the attenuation increases as the square root of frequency; see [b-Bell Tx] and [b-Wiggington] for details) and the loss at a frequency of 17 184 kHz shall be in the range 0 to 12 dB.

For the jitter to be tolerated at the input port, refer to clause 7.1.4 of [ITU-T G.823].

The return loss at the input port should have the provisional minimum values given in Table 13-3:

Table 13-3 – Digital interface at 34 368 kbit/s input port minimum return loss

Frequency range (kHz)	Return loss (dB)
860 to 1720 1720 to 34 368 34 368 to 51 550	12 18 14

To ensure adequate immunity against signal reflections that can arise at the interface due to impedance irregularities at digital distribution frames and at digital output ports, input ports are required to meet the following requirement:

A nominal aggregate signal, encoded into HDB3 and having a pulse shape as defined in the pulse mask shall have added to it an interfering signal with the same pulse shape as the wanted signal. The interfering signal should have a bit rate within limits specified in this Recommendation, but should not be synchronous with the wanted signal. The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance 75 ohms to give a signal-to-interference ratio of 20 dB. The binary content of the interfering signal should comply with [ITU-T O.151] (2^{23} – 1 bit period). No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the input port.

13.4 Grounding of outer conductor

The outer conductor of the coaxial pair shall be connected to the bonding network both at the input port and the output port.

NOTE 1 – The cable routing is important if leaving the system block. Consult [ITU-T K.27] for guidance.

NOTE 2 – The use of isolation to the bonding network is for further study.

14 Interface at 139 264 kbit/s (E4)

14.1 General characteristics

Nominal bit rate: 139 264 kbit/s.

Bit rate accuracy: ±15 ppm (±2089 bit/s).

Code: Coded mark inversion (CMI) (a description of this code can be found in Annex A).

Overvoltage protection requirements: refer to [ITU-T K.20].

14.2 Specifications at the output ports

The specifications at the output ports are given in Table 14-1 and Figures 14-1 and 14-2. See also Note 6 of clause 1.

NOTE – A method based on the measurement of the levels of the fundamental frequency component, the second (and possibly the third) harmonic of a signal corresponding to binary all 0s and binary all 1s, is considered to be a perfectly adequate method of checking that the requirements of Table 14-1 have been met. The relevant values of the harmonic components are under study.

Table 14-1 – Digital interface at 139 264 kbit/s

Parameter	Specification
Pulse shape	Nominally rectangular and conforming to the masks shown in Figures 14-1 and 14-2
Pair(s) in each direction	One coaxial pair
Test load impedance	75 ohms resistive
Peak-to-peak voltage	1 ± 0.1 V
Rise time between 10% and 90% amplitudes of the measured steady state amplitude	≤2 ns
Transition timing tolerance (referred to the mean value of the 50% amplitude points of negative transitions)	Negative transitions: ±0.1 ns Positive transitions at unit interval boundaries: ±0.5 ns Positive transitions at mid-interval: ±0.35 ns
Return loss	≥15 dB over frequency range 7 MHz to 210 MHz
Maximum peak-to-peak jitter at an output port	Refer to clause 5.1 of [ITU-T G.823]

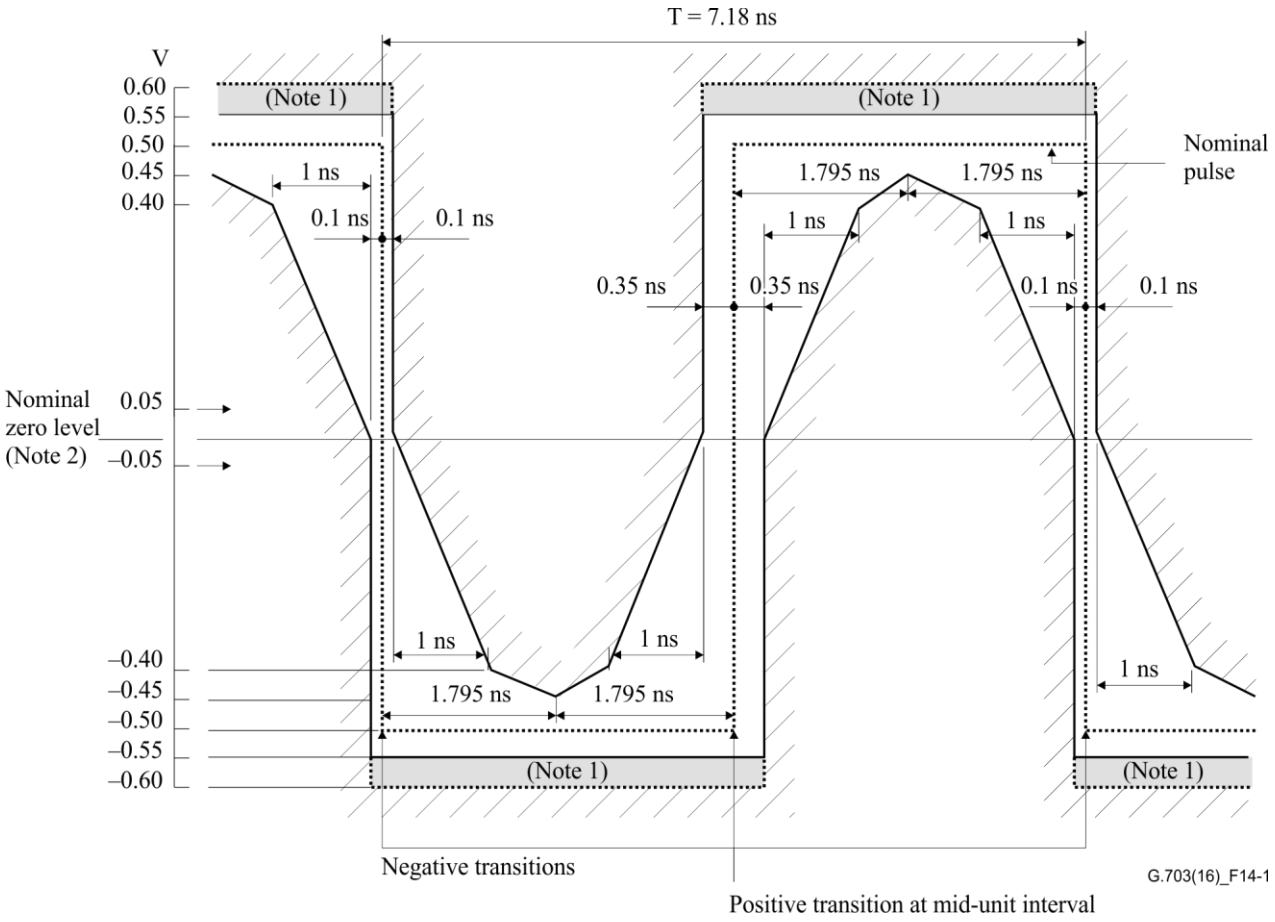


Figure 14-1 – Mask of a pulse corresponding to a binary 0 at the 139 264 kbit/s interface

NOTE 1 – The maximum "stead state" amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V, provided that they do not exceed the steady state level by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

NOTE 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 µF, to the input of the oscilloscope used for measurements.

The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ±0.05 V of the nominal zero level of the masks.

NOTE 3 – Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e., with their nominal start and finish edges coincident.

The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal.

When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques (e.g., a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal).

These techniques require further study.

NOTE 4 – For the purpose of these masks, the rise time and decay time should be measured between −0.4 V and 0.4 V, and should not exceed 2 ns.

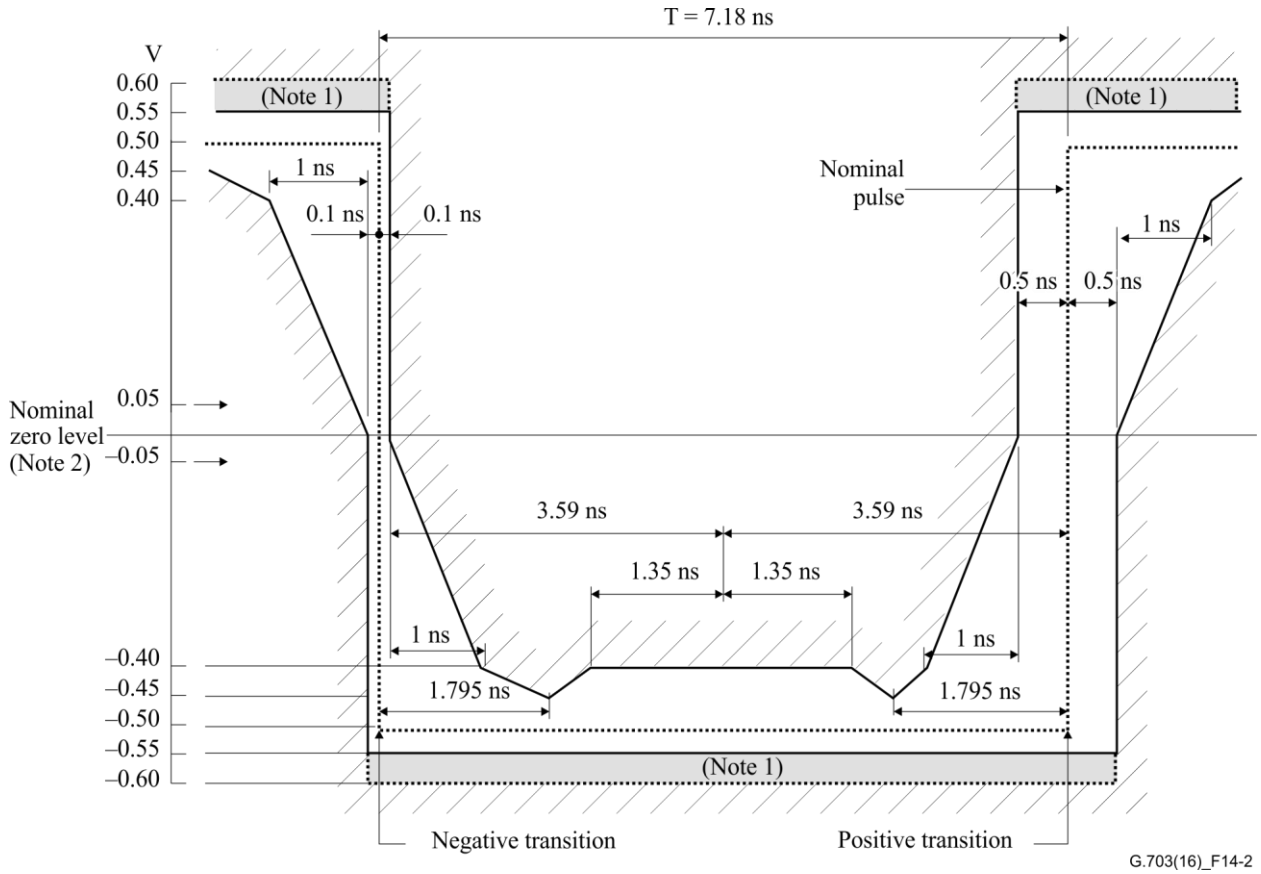


Figure 14-2– Mask of a pulse corresponding to a binary 1 at the 139 264 kbit/s interface

NOTE 1 – The maximum "stead state" amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V, provided that they do not exceed the steady state level by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

NOTE 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 µF, to the input of the oscilloscope used for measurements.

The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ±0.05 V of the nominal zero level of the masks.

NOTE 3 – Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e., with their nominal start and finish edges coincident.

The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal.

When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques (e.g., a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal).

These techniques require further study.

NOTE 4 – For the purpose of these masks, the rise time and decay time should be measured between −0.4 V and 0.4 V, and should not exceed 2 ns.

NOTE 5 – The inverse pulse will have the same characteristics, noting that the timing tolerance at the level of the negative and positive transitions are ±0.1 ns and ±0.5 ns respectively.

14.3 Specifications at the input ports

The digital signal presented at the input port should conform to Table 14-1 and Figures 14-1 and 14-2 modified by the characteristics of the interconnecting coaxial pair.

The attenuation of the coaxial pair should be assumed to follow an approximate $\sqrt{f}$ law (i.e., the attenuation increases as the square root of frequency; see [b-Bell Tx] and [b-Wiggington] for details) and to have a maximum insertion loss of 12 dB at a frequency of 70 MHz.

For the jitter to be tolerated at the input port, refer to clause 7.1.5 of [ITU-T G.823].

The return loss characteristics should be the same as that specified for the output port.

14.4 Grounding of outer conductor

The outer conductor of the coaxial pair shall be connected to the bonding network both at the input port and the output port.

NOTE 1 – The cable routing is important if leaving the system block. Consult [ITU-T K.27] for guidance.

NOTE 2 – The use of isolation to the bonding network is for further study.

15 2048 kHz synchronization interface (T12)

15.1 General characteristics

The use of this interface is recommended for all applications where it is required to synchronize a digital equipment by an external 2048 kHz synchronization signal.

Overvoltage protection requirements: refer to [ITU-T K.20].

15.2 Specifications at the output ports

For general characteristics, see Table 15-1; for frequency accuracy requirements, see Table 15-2. See also Note 6 of clause 1.

Table 15-1 – Digital 2048 kHz clock interface

Parameter	Specification	
Pulse shape	The signal must conform with the mask (Figure 15-1). The value V corresponds to the maximum peak value. The value V_1 corresponds to the minimum peak value.	
Type of pair	Coaxial pair (see Note in clause 13.4)	Symmetrical pair (see Note in clause 13.4)
Test load impedance	75 ohms resistive	120 ohms resistive
Maximum peak voltage (V)	1.5 V	1.9 V
Minimum peak voltage (V_1)	0.75 V	1.0 V
Maximum jitter at an output port	Refer to Table 5 in [ITU-T G.823] (Note)	
NOTE – This value is valid for network timing synchronization equipment. Other values may be specified for timing output ports of digital links carrying the network timing.		

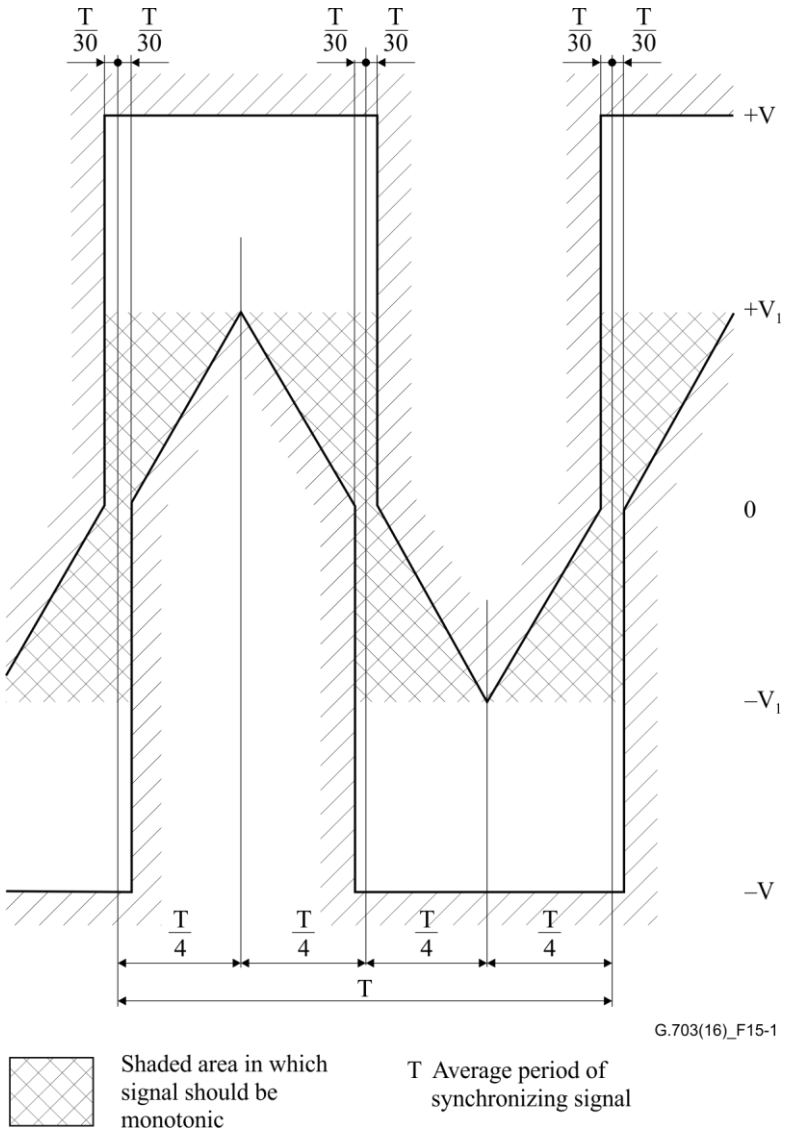


Figure 15-1 – Wave shape at an output port of the 2048 kHz synchronization interface

Table 15-2 – Digital 2048 kHz clock – Frequency accuracy at output ports

Output interface	Required accuracy
Primary reference clock – PRC	Refer to [ITU-T G.811]
Synchronization supply unit – SSU	Refer to [ITU-T G.812]
SDH equipment clock – SEC	4.6 ppm; refer also to [ITU-T G.813]
Synchronization interfaces used in legacy applications (e.g., PDH)	±50 ppm

15.3 Specifications at the input ports

The signal presented at the input ports should be as defined above but modified by the characteristics of the interconnecting pair.

The attenuation of this pair shall be assumed to follow a $\sqrt{f}$ law (i.e., the attenuation increases as the square root of frequency; see [b-Bell Tx] and [b-Wiggington] for details) and the loss at a frequency of 2048 kHz should be in the range 0 to 6 dB (minimum value). This attenuation should take into account any losses incurred by the presence of a digital distribution frame between the equipment.

The input port shall be able to tolerate a digital signal with these electrical characteristics but modulated by jitter. See Table 15-3.

The return loss at 2048 kHz should be ≥15 dB.

Table 15-3 – Digital 2048 kHz clock – Noise tolerance at input ports

Input interface	Jitter tolerance
Primary reference clock – PRC	Not applicable
Synchronization supply unit – SSU	Refer to [ITU-T G.812]
SDH equipment clock – SEC	Refer to [ITU-T G.813]
Synchronization interfaces used in legacy applications (e.g., PDH)	For further study

15.4 Grounding of outer conductor or screen

The outer conductor of the coaxial pair or the screen of the symmetrical pair shall be connected to the bonding network both at the input port and the output port.

NOTE 1 – The cable routing is important if leaving the system block. Consult [ITU-T K.27] for guidance.

NOTE 2 – The use of isolation to the bonding network is for further study.

16 Interface at 97 728 kbit/s

Interconnection of 97 728 kbit/s signals for transmission purposes is accomplished at a digital distribution frame.

Nominal bit rate: 97 728 kbit/s.

Bit rate accuracy: ±10 ppm (±978 bit/s).

One coaxial pair shall be used for each direction of transmission.

The test load impedance shall be 75 ohms ± 5% resistive.

A scrambled AMI code[1] shall be used.

The shape for the 97 728 kbit/s output port shall fall within the mask in Figure 16-1. The shape at the point where the signal arrives at the distribution frame will be modified by the characteristics of the interconnecting cable.

[1] An AMI code is scrambled by a five-stage reset-type scrambler with the primitive polynomial of $x^5 + x^3 + 1$.

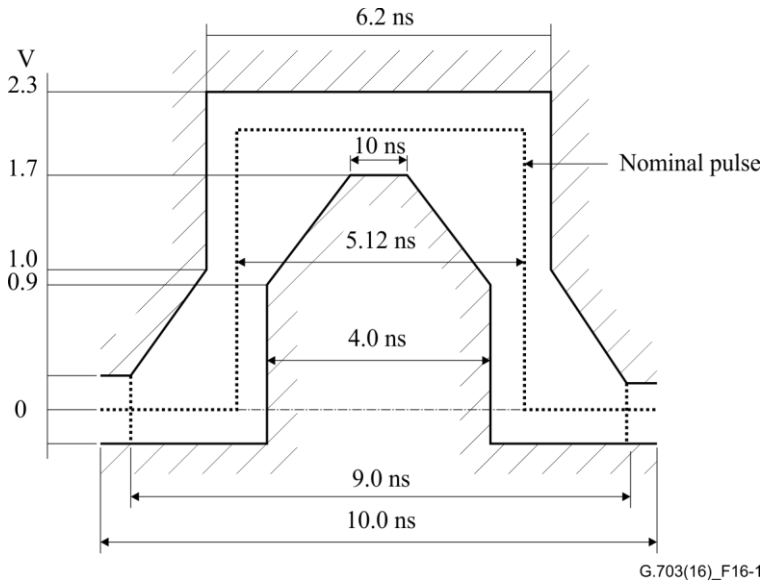


Figure 16-1 – Pulse mask at the 97 728 kbit/s output port

The connectors and cable pairs in the distribution frame shall be 75 ohms ±5%.

Jitter requirements:

– For the maximum peak-to-peak jitter at the output port, refer to clause 5.1 of [ITU-T G.824];

– For the jitter to be tolerated at the input port, refer to clause 7.2.5 of [ITU-T G.824].

Overvoltage protection requirements: refer to [ITU-T K.20].

17 Interface at 155 520 kbit/s – STM-1 interface (ES1)

17.1 General characteristics

Nominal bit rate: 155 520 kbit/s.

Bit rate accuracy: ±20 ppm (±3111 bit/s).

Code: Coded mark inversion (CMI) (a description of this code can be found in Annex A).

Overvoltage protection requirements: refer to [ITU-T K.20].

17.2 Specifications at the output ports

The specifications at the output ports are given in Table 17-1 and in Figures 17-1 and 17-2. See also Note 6 of clause 1.

NOTE – A method based on the measurement of the levels of the fundamental frequency component, the second (and possibly the third) harmonic of a signal corresponding to the binary all 0s and binary all 1s, is considered to be a perfectly adequate method of checking that the requirements of Table 17-1 have been met. The relevant values of the harmonic components are under study.

Table 17-1 – Digital interface at 155 520 kbit/s

Parameter	Specification
Pulse shape	Nominally rectangular and conforming to the masks shown in Figures 17-1 and 17-2
Pair(s) in each direction	One coaxial pair
Test load impedance	75 ohms resistive
Peak-to-peak voltage	1 ± 0.1 V
Rise time between 10% and 90% amplitudes of the measured steady state amplitude	≤2 ns
Transition timing tolerance referred to the mean value of the 50% amplitude points of negative transitions	Negative transitions: ±0.1 ns Positive transitions at unit interval boundaries: ±0.5 ns Positive transitions at mid-unit intervals: ±0.35 ns
Return loss	≥15 dB over frequency range 8 MHz to 240 MHz
Maximum peak-to-peak jitter at an output port	Refer to clause 5.1 of [ITU-T G.825]

17.3 Specifications at the input ports

The digital signal presented at the input port should conform to Table 17-1 and Figures 17-1 and 17-2 modified by the characteristics of the interconnecting coaxial pair.

The attenuation of the coaxial pair should be assumed to follow an approximate $\sqrt{f}$ law (i.e., the attenuation increases as the square root of frequency; see [b-Bell Tx] and [b-Wiggington] for details) and to have a maximum insertion loss of 12.7 dB at a frequency of 78 MHz.

For the jitter to be tolerated at the input port, refer to clause 6.1.2.1 of [ITU-T G.825].

The return loss characteristics should be the same as that specified for the output port.

17.4 Specifications at the cross-connect points

– Signal power level: A wideband power measurement using a power level sensor with a working frequency range of at least 300 MHz shall be between −2.5 and +4.3 dBm. There shall be no DC power transmitted across the interface.

– Eye diagram: An eye diagram mask based on the maximum and minimum power levels given above is shown in Figure 17-3 where the voltage amplitude has been normalized to one, and the time scale is specified in terms of the pulse repetition period T. The corner points of the eye diagram are shown in Figure 17-3.

– Termination: One coaxial cable shall be used for each direction of transmission.

– Impedance: A resistive test load of 75 ohms ±5% shall be used at the interface for the evaluation of the eye diagram and the electrical parameters of the signal.

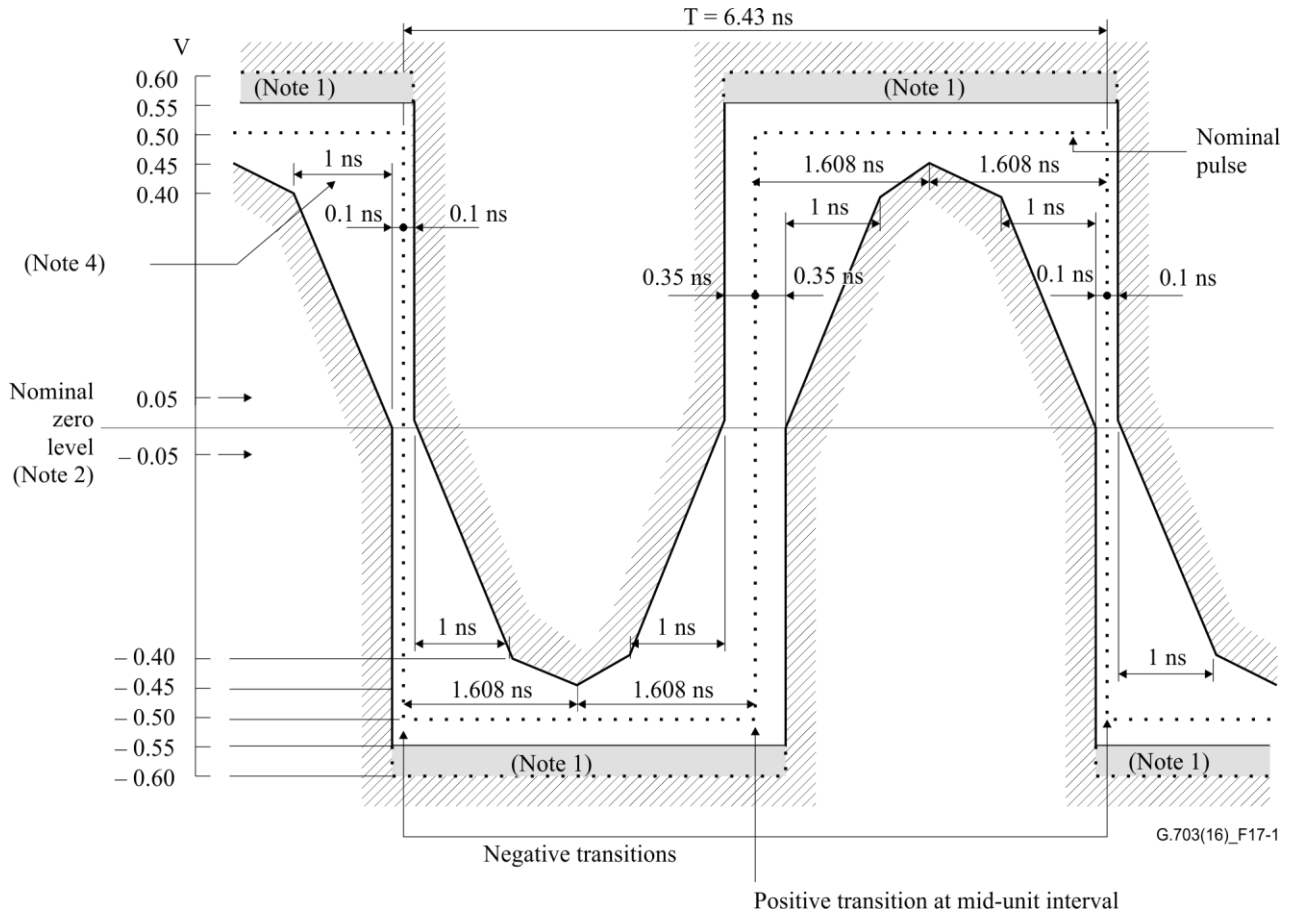


Figure 17-1 – Mask of a pulse corresponding to a binary 0 (at the 155 520 kbit/s interface)

NOTE 1 – The maximum "stead state" amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V, provided that they do not exceed the steady state level by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

NOTE 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 µF, to the input of the oscilloscope used for measurements.

The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ±0.05 V of the nominal zero level of the masks.

NOTE 3 – Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e., with their nominal start and finish edges coincident.

The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal.

When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques (e.g., a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal).

These techniques require further study.

NOTE 4 – For the purpose of these masks, the rise time and decay time should be measured between −0.4 V and 0.4 V, and should not exceed 2 ns.

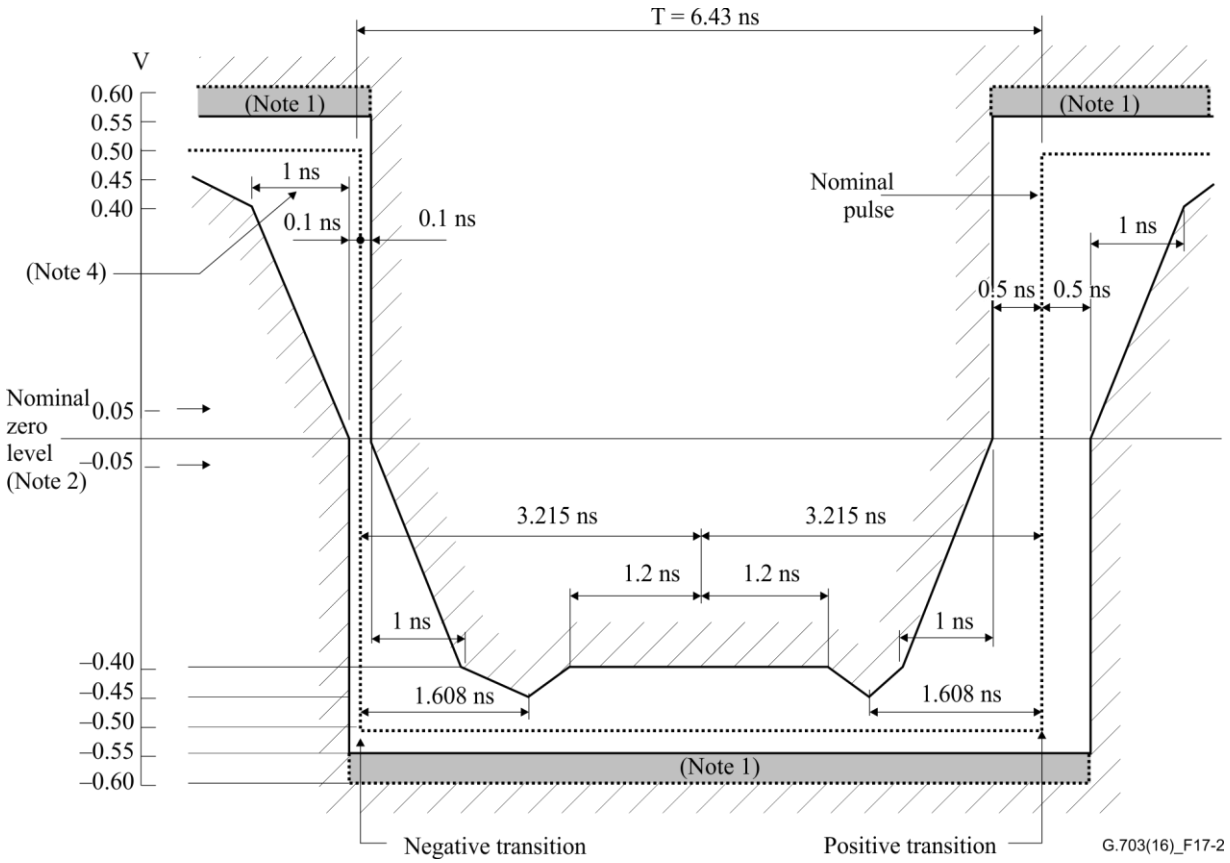


Figure 17-2 – Mask of a pulse corresponding to a binary 1 (at the 155 520 kbit/s interface)

NOTE 1 – The maximum "stead state" amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V, provided that they do not exceed the steady state level by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

NOTE 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 µF, to the input of the oscilloscope used for measurements.

The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ±0.05 V of the nominal zero level of the masks.

NOTE 3 – Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e., with their nominal start and finish edges coincident.

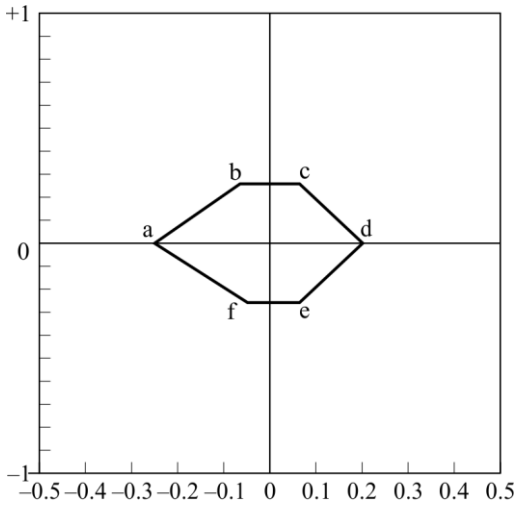
The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal.

When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques (e.g., a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal).

These techniques require further study.

NOTE 4 – For the purpose of these masks, the rise time and decay time should be measured between −0.4 V and 0.4 V, and should not exceed 2 ns.

NOTE 5 – The inverse pulse will have the same characteristics, noting that the timing tolerance at the level of the negative and positive transitions are ±0.1 ns and ±0.5 ns respectively.



Point	Time	Amplitude
a	$-0.25\frac{T}{2}$	0.00
b	$-0.05\frac{T}{2}$	+0.25
c	$+0.05\frac{T}{2}$	+0.25
d	$+0.20\frac{T}{2}$	0.00
e	$+0.05\frac{T}{2}$	–0.25
f	$-0.05\frac{T}{2}$	–0.25

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Figure 17-3 – STM-1 interface eye diagram

17.5 Grounding of outer conductor

The outer conductor of the coaxial pair shall be connected to the bonding network both at the input port and the output port.

NOTE 1 – The cable routing is important if leaving the system block. Consult [ITU-T K.27] for guidance.

NOTE 2 – The use of isolation to the bonding network is for further study.

18 Interface at 51 840 kbit/s (STM-0 interface)

18.1 General characteristics

Nominal bit rate: 51 840 kbit/s.

Bit rate accuracy: ±20 ppm (±1037 bit/s).

Code – Three line codes may be used:

a) Coded mark inversion (CMI);

b) High density bipolar of order 2 (HDB2) code;

c) High density bipolar of order 3 (HDB3) code.

A description of these codes can be found in Annex A.

Overvoltage protection requirements: refer to [ITU-T K.20].

18.2 Specifications at the output ports

The specifications at the output ports are given in Table 18-1. See also Note 6 of clause 1.

Table 18-1 – Digital interface at 51 840 kbit/s

Parameter	Specifications
Pair(s) in each direction	One coaxial pair
Test load impedance	75 ohms resistive
Maximum peak-to-peak jitter at an output port	1.5 UIpp in the bandwidth from 100 Hz to 400 kHz 0.15 UIpp in the bandwidth from 20 kHz to 400 kHz NOTE 1 – The high-pass measurement filters have a first-order characteristic and a roll-off of −20 dB/decade. The low-pass measurement filters have a maximally flat, Butterworth characteristic and a roll-off of −60 dB/decade. NOTE 2 –The values of jitter for CMI coded STM-0 signals are provisional and should be studied.
If HDB2 or HDB3 codes are used:	
Pulse shape	Nominally rectangular and conforming to the mask (Figure 18-1) irrespective of the sign. The value V corresponds to the nominal peak value.
Nominal peak voltage of a mark (pulse)	1.0 V
Peak voltage of a space (no pulse)	0 V ± 0.1 V
Nominal pulse width	9.65 ns
Ratio of the amplitudes of positive and negative pulses at the center of a pulse interval	0.95 to 1.05
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05
If CMI code is used:	
Pulse shape	Nominally rectangular and conforming to the masks shown in Figures 18-2 and 18-3
Peak-to-peak voltage	1 ± 0.1 V
Rise time between 10% and 90% amplitudes of the measured steady state amplitude	≤6 ns
Transition timing tolerance referred to the mean value of the 50% amplitude points of negative transitions	Negative transitions: ±0.3 ns Positive transitions at unit interval boundaries: ±1.5 ns Positive transitions at mid-unit intervals: ±1 ns

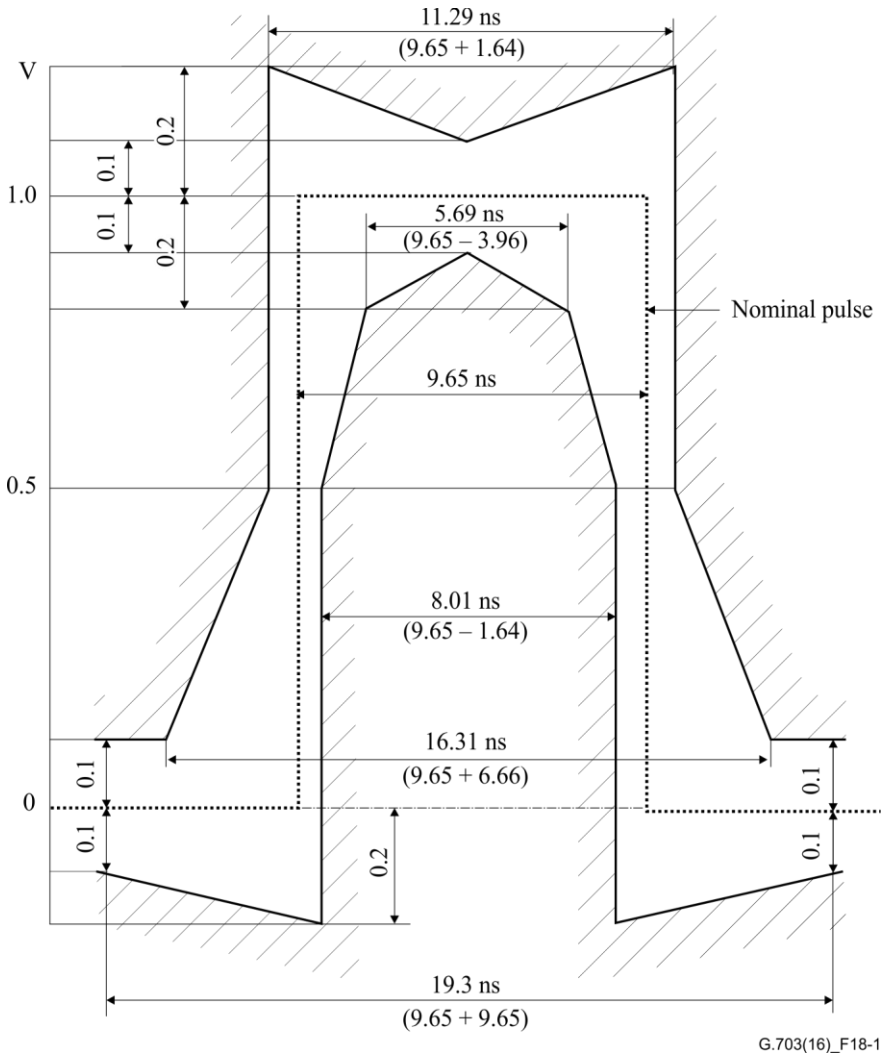


Figure 18-1 – Pulse mask at the 51 840 kbit/s interface (if HDB2 or HDB3 codes are used)

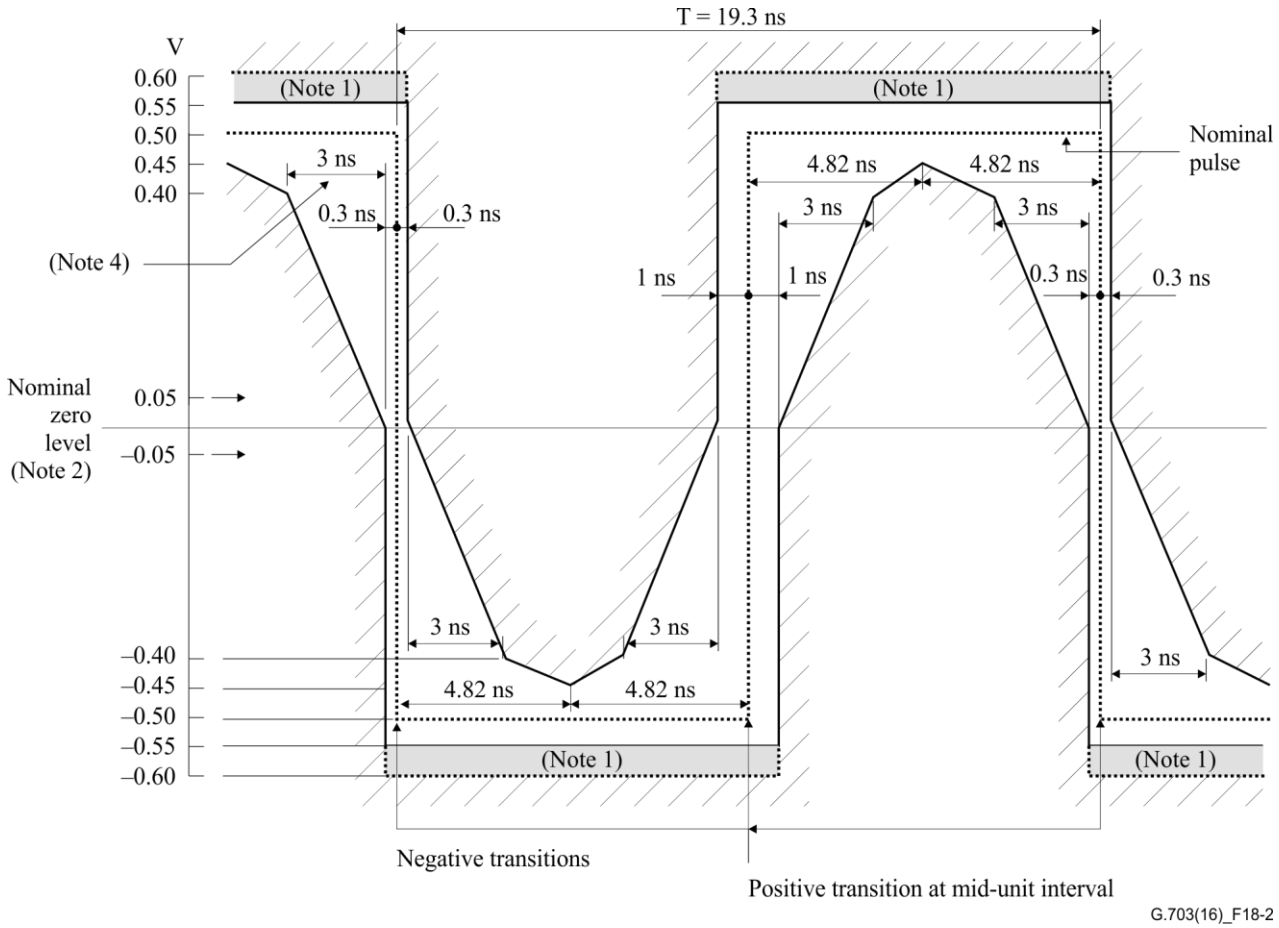


Figure 18-2 – Mask of a pulse corresponding to a binary 0 (at the 51 840 kbit/s interface)

NOTE 1 – The maximum "stead state" amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V, provided that they do not exceed the steady state level by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

NOTE 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01µF, to the input of the oscilloscope used for measurements.

The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ±0.05 V of the nominal zero level of the masks.

NOTE 3 – Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e., with their nominal start and finish edges coincident.

The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal.

When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques (e.g., a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal).

These techniques require further study.

NOTE 4 – For the purpose of these masks, the rise time and decay time should be measured between −0.4 V and 0.4 V, and should not exceed 6 ns.

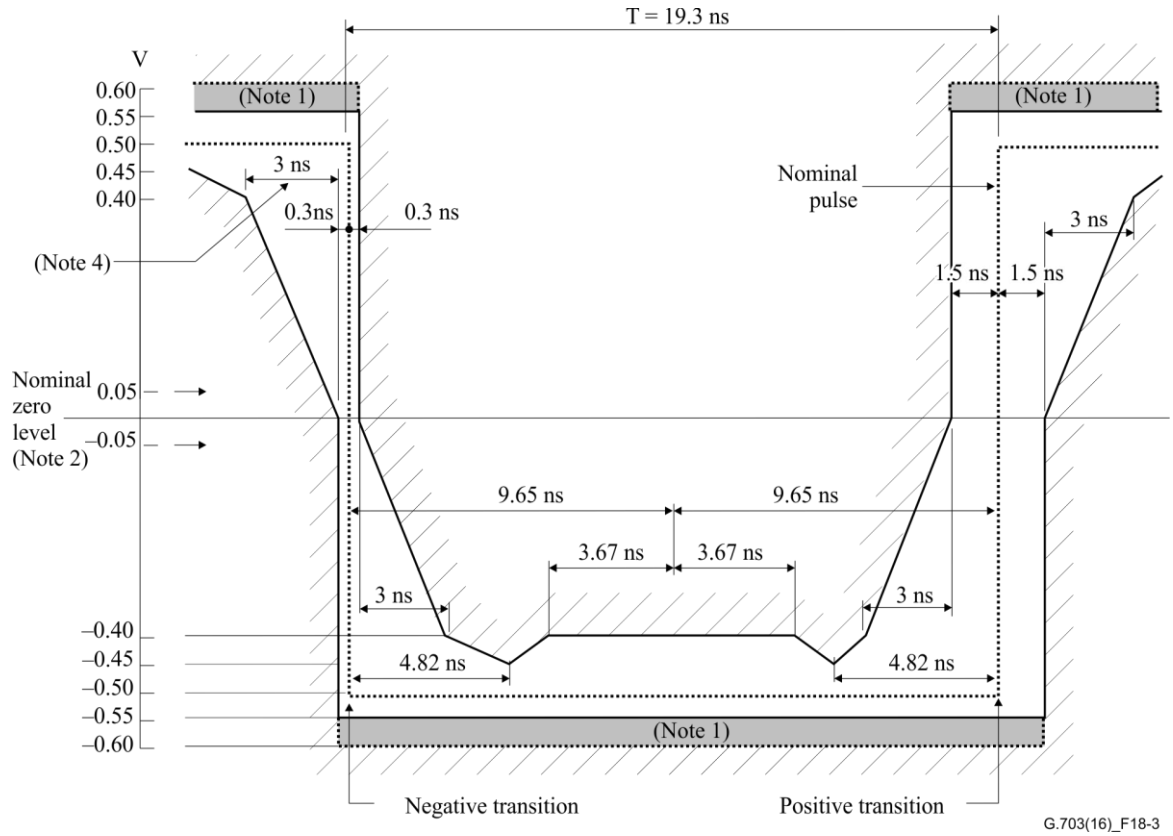


Figure 18-3 – Mask of a pulse corresponding to a binary 1 (at the 51 840 kbit/s interface)

NOTE 1 – The maximum "stead state" amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V, provided that they do not exceed the steady state level by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

NOTE 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01µF, to the input of the oscilloscope used for measurements.

The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ±0.05 V of the nominal zero level of the masks.

NOTE 3 – Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e., with their nominal start and finish edges coincident.

The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal.

When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques (e.g., a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal).

These techniques require further study.

NOTE 4 – For the purpose of these masks, the rise time and decay time should be measured between −0.4 V and 0.4 V, and should not exceed 6 ns.

NOTE 5 – The inverse pulse will have the same characteristics, noting that the timing tolerance at the level of the negative and positive transitions are ±0.3 ns and ±1.5 ns respectively.

The return loss at the output port should have the minimum values given in Table 18-2:

Table 18-2 – Digital interface at 51 840 kbit/s output port minimum return loss

Frequency range (kHz)	Return loss (dB)
1296 to 2592 2592 to 77 760	6 8

18.3 Specifications at the input ports

The digital signal presented at the input port shall be as defined above but modified by the characteristics of the interconnecting pair. The attenuation of this cable shall be assumed to follow approximately a $\sqrt{f}$ law (i.e., the attenuation increases as the square root of frequency; see [b-Bell Tx] and [b-Wiggington] for details) and the loss at a frequency of 25 920 kHz shall be in the range from 0 to 12 dB.

The return loss at the input port should have the provisional minimum values given in Table 18-3:

Table 18-3 – Digital interface at 51 840 kbit/s input port minimum return loss

Frequency range (kHz)	Return loss (dB)
1296 to 2592 2592 to 51 840 51 840 to 77 760	12 18 14

The jitter to be tolerated at the input port expressed in peak-to-peak sinusoidal phase amplitude, shall exceed the values shown in Figure 18-4:

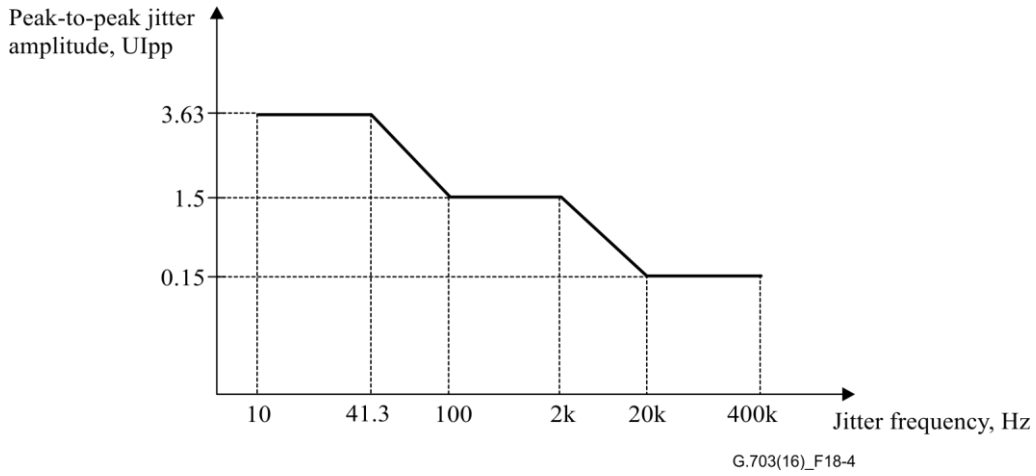


Figure 18-4 – 51 840 kbit/s input jitter tolerance limit

NOTE – The values of jitter for CMI coded STM-0 signals are provisional and should be studied.

18.4 Specifications at the cross-connect points

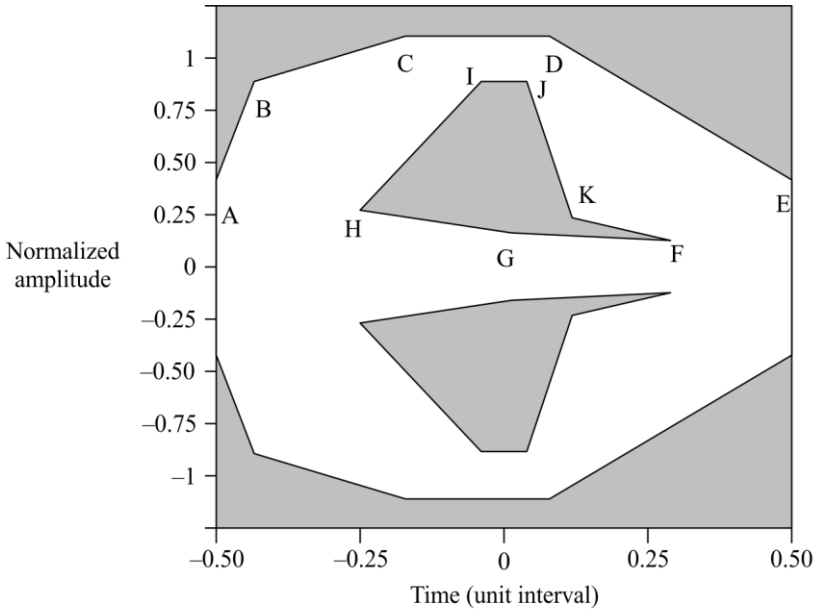
– Signal power level

A wideband power measurement using a power level sensor with a working frequency range of at least four times the bit rate frequency shall be between −2.7 and +4.7 dBm, accounting for both transmitter variations and a range of connecting cable lengths between 68.6 m and 137 m. A filter with a characteristic equivalent to a Butterworth low pass filter with a cut-off frequency of 207.360 MHz shall be used.

There shall be no DC power transmitted across the interface.

– Eye diagram

An eye diagram mask based on the maximum and minimum power levels and cable lengths given above is shown in Figure 18-5 where the voltage amplitude has been normalized to one, and the time scale is specified in terms of the unit interval T. Exclusionary regions are shown as shaded areas on the figure. The corner points of these regions are listed below the figure.



Outer region corner points			Inner region corner points		
Point	**Time**	**Amplitude**	**Point**	**Time**	**Amplitude**
A	–0.50	0.37	F	0.28	0.12
B	–0.44	0.80	G	0.00	0.16
C	–0.18	1.00	H	–0.25	0.24
D	0.08	1.00	I	–0.04	0.80
E	0.50	0.37	J	0.04	0.80
			K	0.11	0.22

NOTE – Both inner and outer regions are symmetric about the zero amplitude axis.

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Figure 18-5 – STM-0 interface eye diagram

18.5 Grounding of outer conductor

The outer conductor of the coaxial pair shall be connected to the bonding network both at the input port and the output port.

NOTE 1 – The cable routing is important if leaving the system block. Consult [ITU-T K.27] for guidance.

NOTE 2 – The use of isolation to the bonding network is for further study.

19 Time synchronization interfaces defined in ITU-T G.8271/Y.1366

19.1 ITU-T V.11-based time/phase distribution interface

The ITU-T V.11-based time/phase distribution interface provides an indication of the time of day and the one pulse per second (1PPS) signal as a phase indication. The expected physical connector is commonly referred to as the RJ-45 connector [IEC 60603-7].

The 1PPS time/phase interface uses a point-to-point [ITU-T V.11] interface as specified in [ITU-T V.11] with an additional requirement on the rise and fall times of the 1PPS signal. This is needed to provide the accuracy required for the 1PPS signal.

This interface can be used for time synchronization distribution as well as for time measurement.

The interface is a balanced interface that can tolerate significant common mode noise.

The 1PPS interface consists of a balanced 100 ohm 1PPS differential signal that can be used to connect to another timing device or to measurement equipment.

The following mapping of signals is defined for use with the RJ-45 connector:

Two modes are supported:

1) Time input mode (the unit receives a time synchronization signal from an external time sync master).
2) Time output mode (the unit outputs a time synchronization signal towards an interface). The receiver of this time sync signal would be a unit operating in time input mode. This could be either test equipment or a time slave clock.

In the event that both time input and time output modes are required at the same time, two RJ-45 connectors are required.

Table 19-1 – RJ-45 connector operating in time input mode

PIN	Signal name	Signal definition
1	Reserved	For further study
2	Reserved	For further study
3	1PPS_IN–	Rx 1PPS negative voltage
4	GND	[ITU-T V.11] signal ground
5	User defined	Note
6	1PPS_IN+	Rx 1PPS positive voltage
7	RX–	Rx TOD time message negative voltage
8	RX+	Rx TOD time message positive voltage
NOTE – One possible use of Pin 5 may be ground (GND). An alternative use for this pin could be considered when connected to GNSS receivers. This is out of the scope of this Recommendation. If the signal is not used, it is recommended to pull it down with a resistor of 10 kΩ.		

Table 19-2 – RJ-45 connector operating in time output mode

PIN	Signal name	Signal definition
1	Reserved	For further study
2	Reserved	For further study
3	1PPS_OUT–	Tx 1PPS negative voltage
4	GND	ITU-T V.11 signal ground
5	GND (Note)	ITU-T V.11 signal ground
6	1PPS_OUT+	Tx 1PPS positive voltage
7	TX–	Tx TOD time message negative voltage
8	TX+	Tx TOD time message positive voltage
NOTE – The time interface discussed in this Recommendation generally concerns transport equipment. For the time output mode interface of a GNSS receiver, similar considerations concerning Pin 5 to those made in the Note to Table 19-1 would be required.		

If only one mode is required, a single RJ-45 can be used and configured as time input or time output mode:

Table 19-3 – RJ-45 connector when only one mode is used

PIN	Signal name – Time input configuration	Signal name – Time output configuration	Signal definition
1	Reserved (Note 1)	Reserved	For further study
2	Reserved (Note 1)	Reserved	For further study
3	1PPS_IN–	1PPS_OUT–	Rx or Tx 1PPS negative voltage
4	GND	GND	ITU-T V.11 signal ground
5	User defined (Note 2)	GND	Note 2
6	1PPS_IN+	1PPS_OUT+	Rx or Tx 1PPS positive voltage
7	RX–	TX–	Rx or Tx TOD time message negative voltage
8	RX+	TX+	Rx or Tx TOD time message positive voltage
NOTE 1 – The use of Pin 1 and Pin 2 is not yet defined. They may be used for the measurement of 1PPS signal delay or may be used for configuring a GNSS receiver unit. Pin 1 and Pin 2 may be differential signals. NOTE 2 – One possible use of Pin 5 in the input configuration may be GND. Alternative usage could be considered when connected to GPS receivers. This is out of the scope of this Recommendation. If the signal is not used, it is recommended to pull it down with a resistor of 10 kΩ.			

19.1.1 1PPS rise and fall time specification

The maximum rise and fall times of the 1PPS_OUT signal pair at the output port are more stringent than those specified in clause 5.3 of [ITU-T V.11]. Values are for further study. The positive pulse width must be between 100 ns and 500 ms.

19.1.2 Signal timing

The time master must generate a positive pulse on the 1PPS signal such that the midpoint of the leading edge of the differential [ITU-T V.11] signal at the edge of the chassis occurs at the change of the one-second time of the system.

The cable delays of the 1PPS signal must be controlled and compensated if needed in the receiving side so as to meet the requirements stated in Table 19-4. This may be done either manually by the network operator or automatically by the equipment.

Table 19-4 – Timing budget for time distribution of the 1PPS interface

Parameter	Tolerance	Reference point
1PPS signal generation accuracy of the timing master	±10 ns	
Cable delay compensation accuracy (Note 1)	±10 ns	From connector to connector with an [ITU-T V.11] pulse
1PPS signal detection accuracy at the slave	Note 2	
NOTE 1 – The applicable cable length is for further study (values between 3 m and 1 000 m have been proposed; contributions are invited). NOTE 2 – A range between 10 and 30 ns has been mentioned, and 30 ns are agreed as worst case. NOTE 3 – The specification of the rise and fall time is for further study.		

19.2 1PPS 50 Ω phase-synchronization measurement interface

The 1PPS interface consists of an unbalanced 50 ohm 1PPS signal that can be used to connect to measurement equipment.

NOTE – The unbalanced 50 ohm 1PPS measurement output may be used for phase distribution assuming that the distribution interface complies with the limits set in Table 19-4. If time distribution is required, an additional interface is required in order to transfer the corresponding time synchronization information. This additional interface is out of the scope of this Recommendation.

As an example, a 1PPS interface consisting of an unbalanced 50 ohm signal has been used as the distribution interface in some legacy equipment that only required phase/frequency synchronization.

19.2.1 Performance specification

This signal indicates the significant event occurring on the midpoint of the leading edge of the signal.

The system must generate a positive pulse on the 1PPS signal such that the midpoint of the leading edge of the signal at the edge of the chassis occurs at the one second roll-over of the system.

The timing specification for the 1PPS measurement interface is shown in Table 19.5.

This interface is intended to be used with an impedance controlled 50 ohm cable with a maximum length of three metres to keep the influence of delay and rise time low.

Table 19-5 – Timing specification for the 1PPS measurement interface

Parameter	Tolerance	Comment
10-90% rise times of the 1PPS pulse	<5 ns	Measured at 1PPS interface
Pulse width	100 ns to 500 ms	Measured at 1PPS interface
Maximum cable length	3 m	Due to delay and rise time performance
NOTE – When the 1PPS output is configured with a simple 50/50 duty cycle, then some allowance to slightly exceed the 500 ms pulse width is permitted. The actual value for this allowance is for further study; a value of 100 ns has been proposed. (As an example, this allowance is to accommodate deviations from precisely 500 ms pulse width that may be due to rise/fall times of clock edges or a duty cycle error of the internal high speed clock that is divided down to create the 1PPS output).		

19.2.2 Voltage levels

Table 19-6 gives voltage levels for the interface for information.

Table 19-6 – Output voltage levels

Interface	VOH (max)	VOH (min)	VOL (max)	VOL (min)
1PPS (50 ohm single-ended)	5.5 V	1.2 V	0.3 V	−0.3 V
NOTE – Measured with a 50 ohm load to ground.				

20 10 MHz synchronization interface

20.1 General characteristics

The use of this interface is recommended for all applications where it is required to synchronize digital equipment by an external 10 MHz synchronization signal.

20.2 Specifications at the output ports

The 10 MHz interface consists of an unbalanced 50 ohm 10 MHz signal that can be used to connect to measurement equipment or other equipment using this synchronization signal.

For general characteristics, see Table 20-1; for frequency accuracy requirements, see Table 20-2. See also Note 6 of clause 1.

Table 20-1 – 10 MHz synchronization interface

Pulse shape	The signal must conform to the mask (Figure 20-1). The value V corresponds to the maximum peak value relative to M. The value V_1 corresponds to the minimum peak value relative to M.
Test load impedance	50 ohms resistive
Maximum peak voltage (V)	2.5 V
Minimum peak voltage (V_1)	0.25 V (Note 4)
Offset voltage (M)	0
Transition region factor (N)	30
Maximum jitter at an output port	(Note 1)
NOTE 1 – For a primary reference 10 MHz output interface of the source clock of the synchronization network, refer to [ITU-T G.811] or [ITU-T G.8272]. Other cases are for further study. NOTE 2 – M is set to 0; non-zero values are for further study. NOTE 3 – N is set to accommodate both sinusoidal and square-wave signals. Equipment can generate any signal that fits within the mask. NOTE 4 – For optimal signal characteristics to be delivered over a cable to the input port, a minimum peak voltage at the output port that is greater than or equal to 0.5 V is recommended. While some equipment designs can accommodate a smaller signal, a stronger signal assures a wide range of equipment, including legacy equipment, can be accommodated.	

Table 20-2 – 10 MHz synchronization interface – Frequency accuracy at output ports

Output interface	Required accuracy
Primary reference clock – PRC	Refer to [ITU-T G.811]
Primary reference time clock - PRTC	Refer to [ITU-T G.8272]
Others	For further study

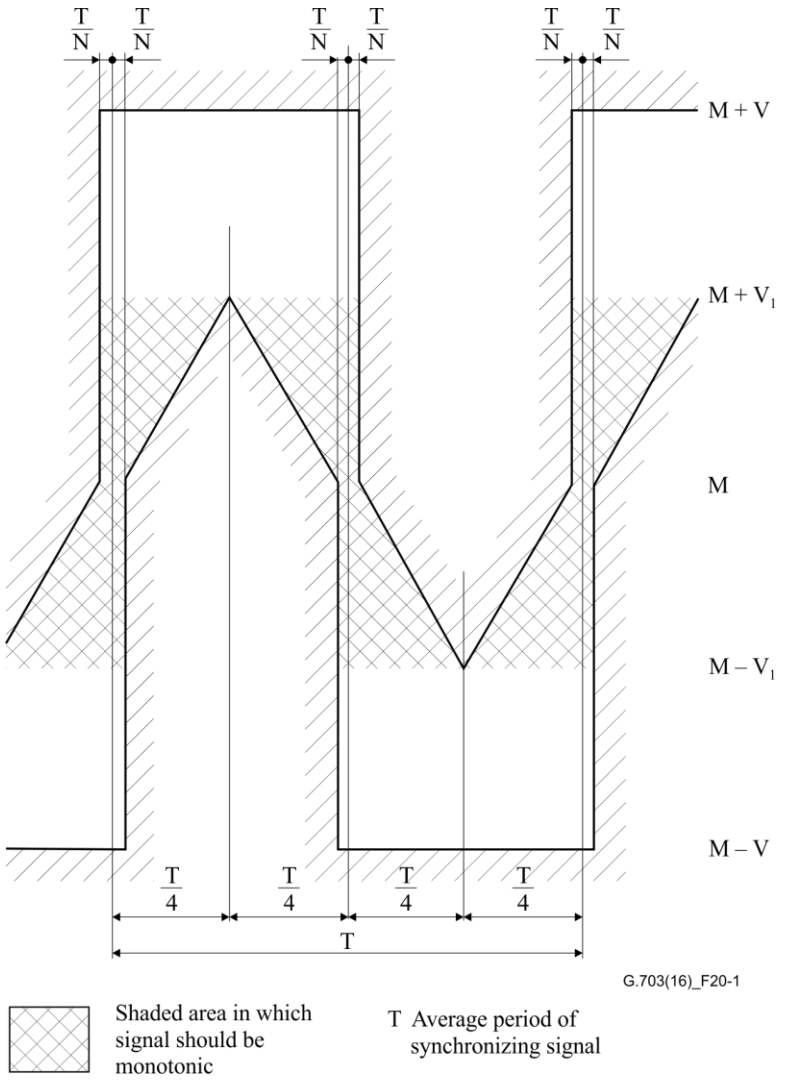


Figure 20-1 – Wave shape at an output port of the 10 MHz synchronization interface

20.3 Specifications at the input ports

The signal presented at the input ports should be as defined above but modified by the characteristics of the interconnecting cable. The attenuation of this cable shall be assumed to follow a $\sqrt{f}$ law (i.e., the attenuation increases as the square root of frequency; see [b-Bell Tx] and [b-Wiggington] for details); the loss at a frequency of 10 MHz should be minimized. The waveshape distortion caused by the cable should also be minimized. This can be achieved by the use of short cable runs, by the use of a low-loss, low-distortion cable, by the use of a strong signal at the originating output port, or by a combination of the above. The maximum allowed attenuation is for further study.

The return loss at 10 MHz should be ≥15 dB.

The input port shall be able to tolerate a signal with these electrical characteristics but modulated by jitter. See Table 20-3.

Table 20-3 – 10 MHz synchronization interface – Noise tolerance at input ports

Input interface	Jitter tolerance
Enhanced primary reference time clock – ePRTC	For further study
Others	For further study

Annex A

Definition of codes

(This annex forms an integral part of this Recommendation.)

This annex defines the modified alternate mark inversion codes (see [ITU-T G.701], item 9005) whose use is specified in this Recommendation.

In these codes, binary 1 bits are generally represented by alternate positive and negative pulses, and binary 0 bits by spaces. Exceptions, as specified for the individual codes, are made when strings of successive 0 bits occur in the binary signal.

In the definitions below, B represents an inserted pulse conforming to the AMI rule (ITU-T G.701, item 9004), and V represents an AMI violation (ITU-T G.701, item 9007).

The encoding of binary signals in accordance with the rules given in this annex includes frame alignment bits, etc.

A.1 Definition of B3ZS (also designated HDB2) and HDB3

Each block of 3 (or 4) successive zeros is replaced by 00V (or 000V respectively) or B0V (B00V). The choice of 00V (000V) or B0V (B00V) is made so that the number of B pulses between consecutive V pulses is odd. In other words, successive V pulses are of alternate polarity so that no DC component is introduced.

A.2 Definition of B6ZS and B8ZS

Each block of 6 (or 8) successive zeros is replaced by 0VB0VB (or 000VB0VB respectively).

A.3 Definition of CMI

CMI is a 2-level non-return-to-zero code in which binary 0 is coded so that both amplitude levels, A_1 and A_2, are attained consecutively, each for half a unit time interval (T/2).

Binary 1 is coded by either of the amplitude levels A_1 or A_2, for one full unit time interval (T), in such a way that the level alternates for successive binary 1s.

An example is given in Figure A.1.

NOTE 1 – For binary 0, there is always a positive transition at the midpoint of the binary unit time interval.

NOTE 2 – For binary 1:

a) there is a positive transition at the start of the binary unit time interval if in the preceding time interval the level was A1;

b) there is a negative transition at the start of the binary unit time interval if the last binary 1 was encoded by level A2.

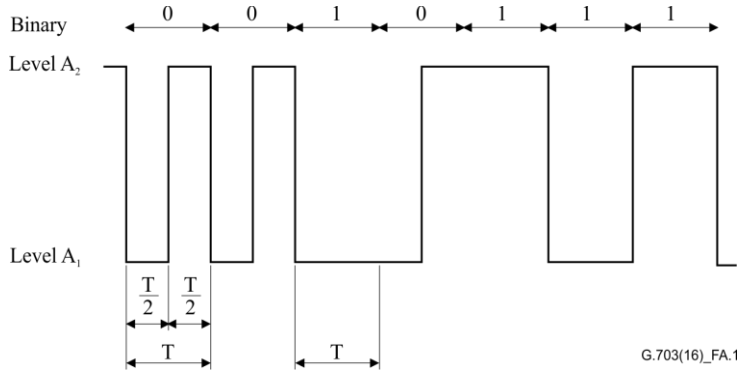


Figure A.1 – Example of CMI coded binary signal

Appendix I

1544 kbit/s specification in the 1991 version of this Recommendation

(This appendix does not form an integral part of this Recommendation.)

I.1 General

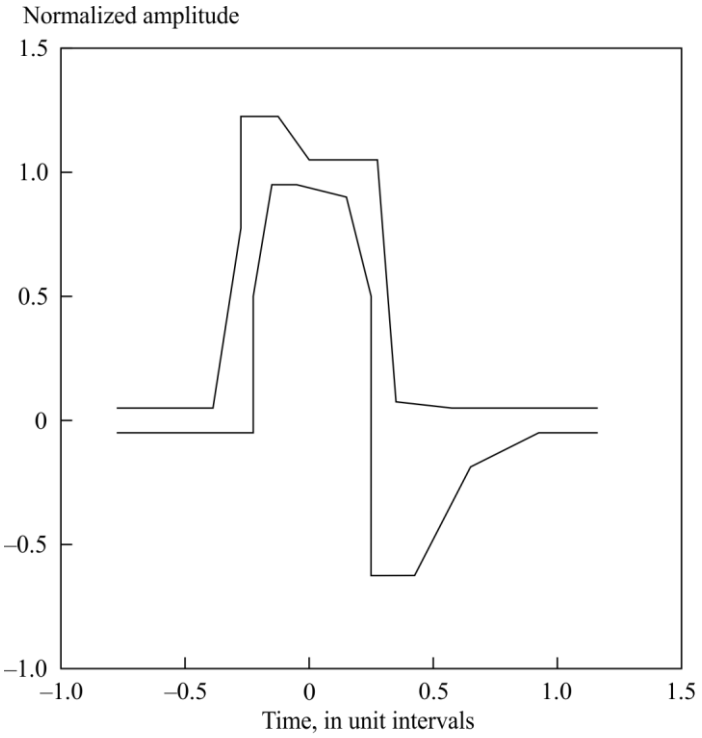
This appendix describes an earlier 1544 kbit/s interface that included a pulse mask with substantially greater allowance for overshoot on the trailing edge of the pulse than the current Recommendation. While the current pulse mask has been socialized in a number of network compatibility publications since the late 1970s, equipment designed to the earlier specification may be widespread in the network. Hence, designers of equipment need to be aware of the nature of signals that may be delivered to that equipment.

I.2 Interface specification

Most of the interface parameters in Table 7-1, including power levels and pulse amplitudes, apply to the older interface. One major difference is in the line rate tolerance. The older specification calls for a ±130 ppm tolerance, reflecting an earlier, now obsolete, technology for line driver circuitry.

I.3 Pulse mask

Figure I.1 is the 1544 kbit/s pulse mask corresponding to the earlier interface specification. It is based on equipment generating pulses with considerably more overshoot on the trailing edge that is currently allowed in the Recommendation.



Minimum curve		Minimum curve	
Time	Normalized amplitude	Time	Normalized amplitude
– 0.77	– 0.05	– 0.77	0.05
– 0.23	– 0.05	– 0.39	0.05
– 0.23	0.5	– 0.27	0.8
– 0.15	0.95	– 0.27	1.22
– 0.04	0.95	– 0.12	1.22
0.15	0.9	0.0	1.05
0.23	0.5	0.27	1.05
0.23	– 0.62	0.34	0.08
0.42	– 0.62	0.58	0.05
0.66	– 0.2	1.16	0.05
0.93	– 0.05		
1.16	– 0.05		

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Figure I.1 – Obsolete 1544 kbit/s interface isolated pulse mask and corner points

Appendix II

64 and 6312 kHz synchronization interface specification for use in Japan

(This appendix does not form an integral part of this Recommendation.)

II.1 64 kHz synchronization interface

The 64 kHz clock signals from the clock supply equipment have the frequencies of:

a) 64 kHz + 8 kHz or

b) 64 kHz + 8 kHz + 400 Hz.

Those signals consist of AMI code with:

a) an 8 kHz bipolar violation, or

b) an 8 kHz bipolar violation removed at every 400 Hz.

The signal structures of 64 kHz clock signals are illustrated in Figures II.1 and II.2.

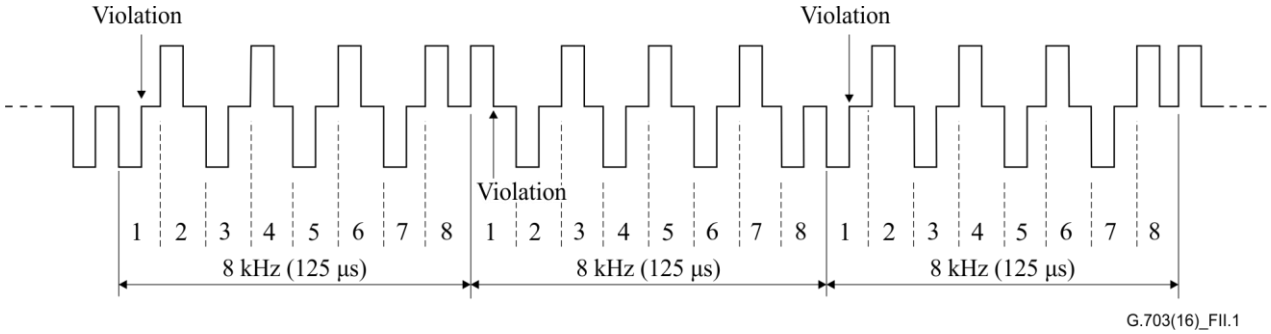

Figure II.1 – Signal structure of 64 kHz clock interface with a frequency of 64 kHz + 8 kHz

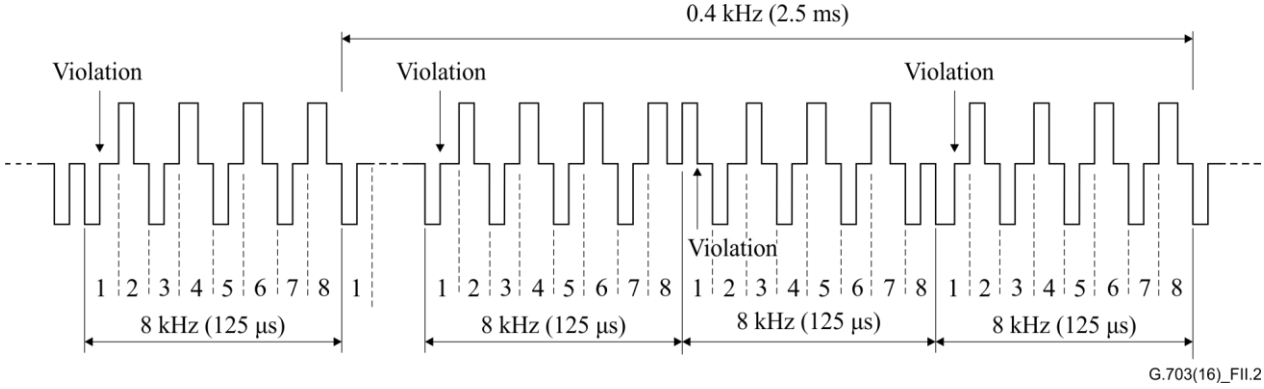

Figure II.2 – Signal structure of 64 kHz clock interface with a frequency of 64 kHz + 8 kHz + 400 Hz

The specifications of 64 kHz clock signals at input port and output port are shown in Tables II.1 and II.2, respectively.

Table II.1 – Specification of 64 kHz clock signal at input port

Frequency	a) 64 kHz + 8 kHz or b) 64 kHz + 8 kHz + 400 Hz
	a) AMI with 8 kHz bipolar violation; b) AMI with 8 kHz bipolar violation removed at every 400 Hz
Alarm condition	Alarm should not be occurred against the amplitude ranged 0.63-1.1 $V_{0\text{-}P}$

Table II.2 – Specification of 64 kHz clock signal at output port

Frequency	a) 64 kHz + 8 kHz or b) 64 kHz + 8 kHz + 400 Hz
Load impedance	110 ohms resistive
Transmission media	Symmetric pair cable
Pulse width (FWHM)	$\leq 7.8 \pm 0.78$ µs
Amplitude	≤ 1 $V_{0\text{-}P} \pm 0.1$ V

II.2 6312 kHz synchronization interface

Figure II.3 shows the waveform of 6312 kHz clock signal. The specifications of 6312 kHz clock signals at input port and output port are shown in Tables II.3 and II.4, respectively.

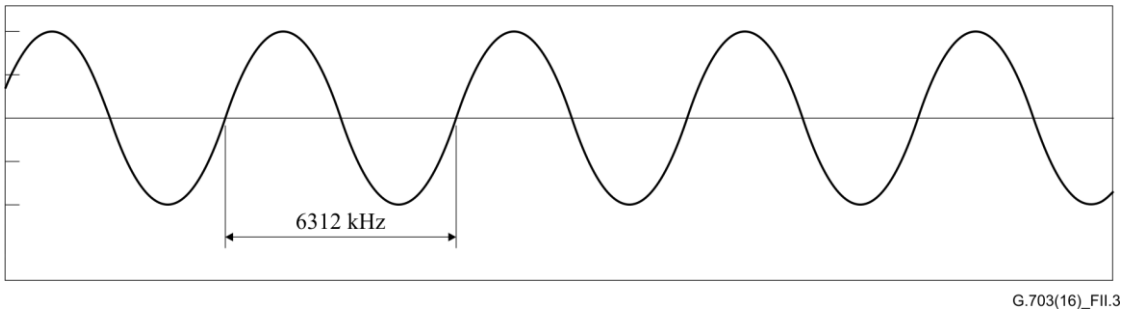

Figure II.3 – Waveform of 6312 kHz clock signal

Table II.3 – Specification of 6312 kHz clock signal at input port

Frequency	6312 kHz
Signal format	Sinusoidal wave
Alarm condition	Alarm should not be occurred against the amplitude ranged −16 dBm to +3 dBm

Table II.4 – Specification of 6312 kHz clock signal at output port

Frequency	6312 kHz
Load impedance	75 ohms resistive
Transmission media	Coaxial pair cable
Amplitude	0 dBm ± 3 dB

Appendix III

3152 kbit/s interface specification for use in North America (From Annex A – [ITU-T G.931)

(This appendix does not form an integral part of this Recommendation.)

Nominal bit rate: 3152 kbit/s.

Bit rate accuracy: ±30 ppm (±95 bit/s).

For specifications at the ports, see Table III.1.

Table III.1 – Digital interface at 3152 kbit/s

Parameter	Specification
Nominal bit rate	3152 kbit/s
Bit rate accuracy	±30 ppm (±95 bit/s)
Test load impedance	100 ohms ± 5% resistive
Line code	AMI (Notes 1 and 2)
Pulse shape	Nominal rectangular
Pair(s) in each direction of transmission	One balanced twisted pair (Note 3)
Nominal amplitude	3.0 V (Note 4)
Width (at 50% amplitude)	159 ± 30 ns
Rise and fall times (20-80% of amplitude)	≤50 ns (difference between rise and fall times shall be 0 ± 20 ns)
Signal power (all is signal, measured over 10 MHz bandwidth)	16.53 ± 2 dBm [ratio of (power in + pulses) to (power in – pulses) shall be 0 ± 0.5 dB]
NOTE 1 – An AMI code shall be used. For definitions of AMI code; see Annex A/[ITU-T G.703]. NOTE 2 – In order to guarantee adequate timing information, the minimum pulse density taken over any 130 consecutive time slots must be 1 in 8. The design intent is that the long-term pulse density be equal to 0.5. In order to provide adequate jitter performance for systems, timing extracting circuits should have a *Q* of 1200 ± 200 that is representable by a single tuned network. NOTE 3 – One balanced twisted pair shall be used for each direction of transmission. The distribution frame jack connected to a pair bringing signals to the distribution frame is termed the in-jack. The distribution frame jack connected to a pair carrying signals away from the distribution frame is termed the out-jack. NOTE 4 – The peak-to-peak voltage within a time slot containing a zero (space) produced by other pulses meeting the specifications of Table III.1 should not exceed 0.1 of the peak pulse amplitude.	

Requirements for the maximum peak-to-peak jitter at the output port and the jitter to be tolerated at the input port are for further study.

Overvoltage protection requirements: refer to [ITU-T K.20].

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