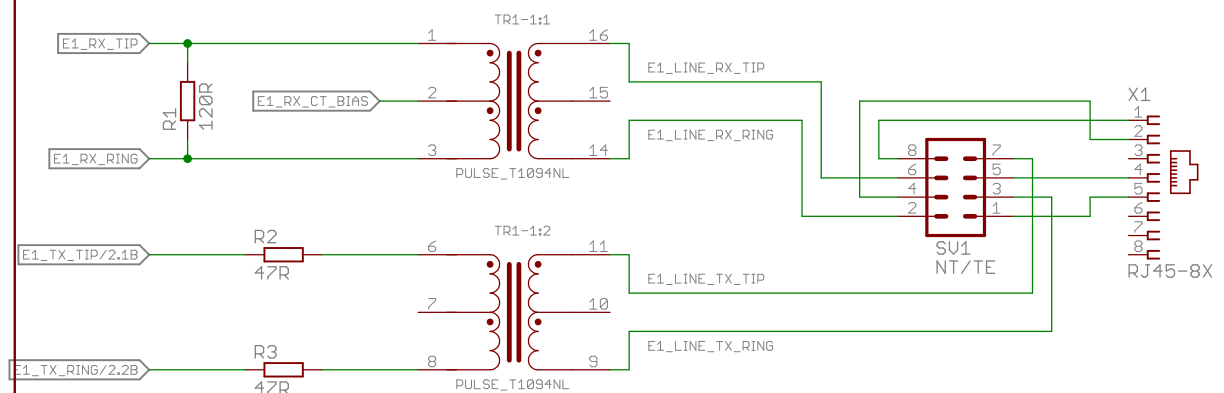
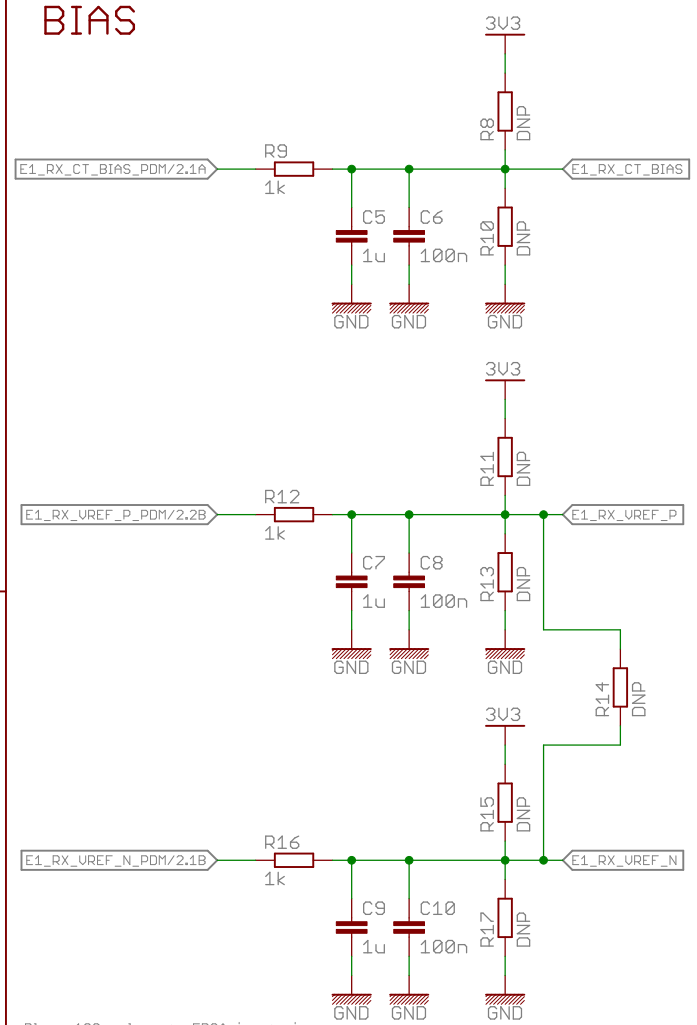


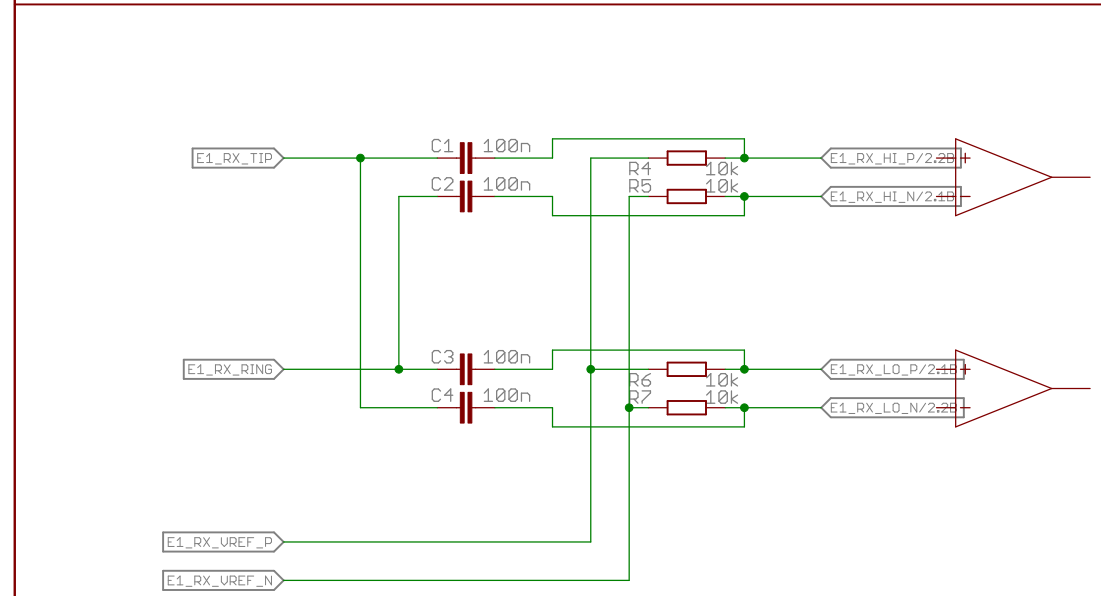
LINE IF



BIAS



Place 100n close to FPGA input pins
Place resistors close to FPGA output pins



RX PHY

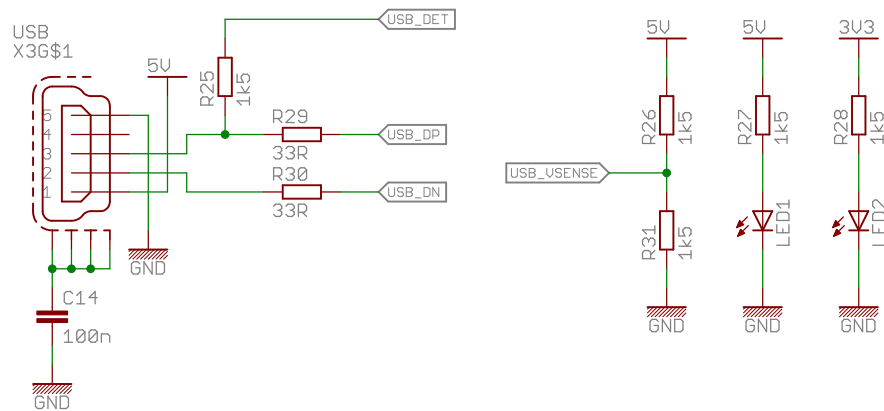
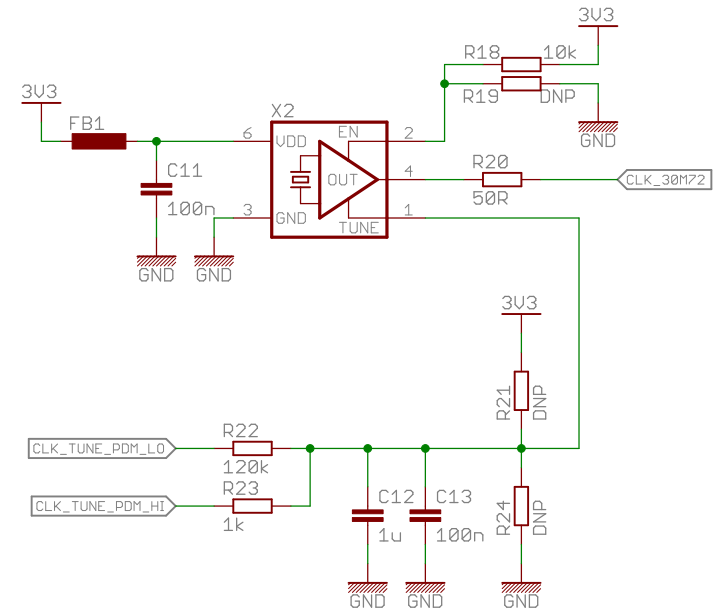
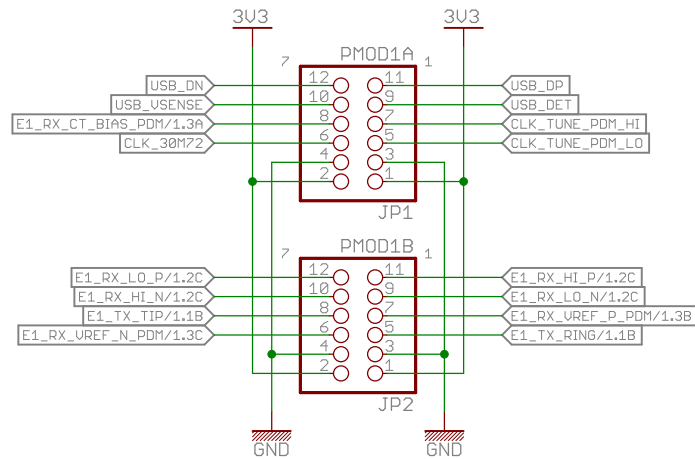
E1 Line interface

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PMOD, USB & Clock

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