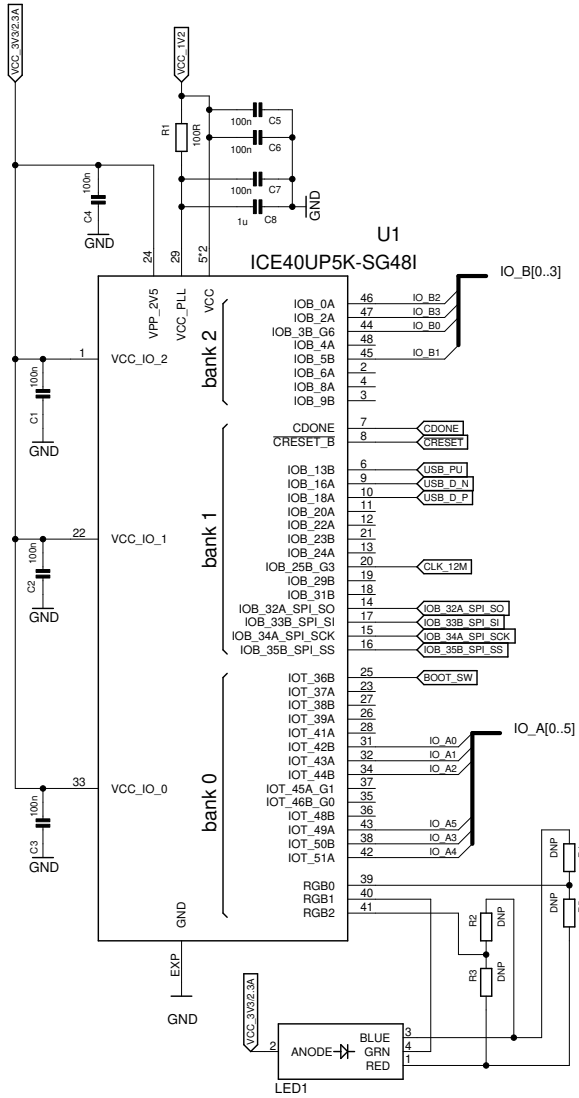
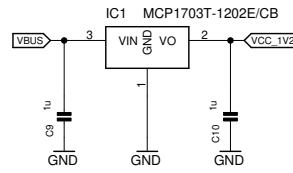


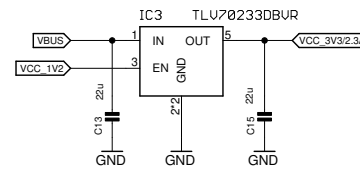
FPGA



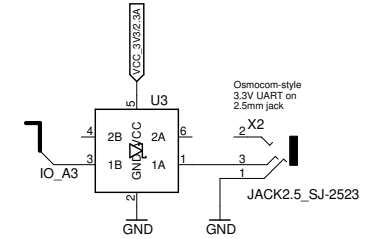
1V2 LDO



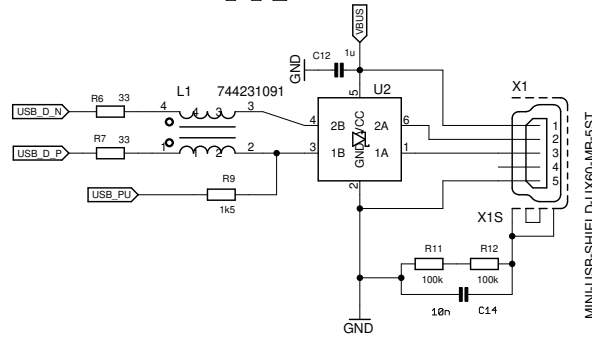
3V3 LDO



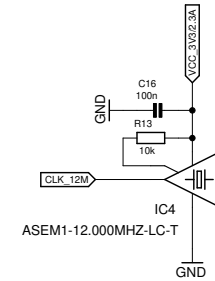
serial debug out



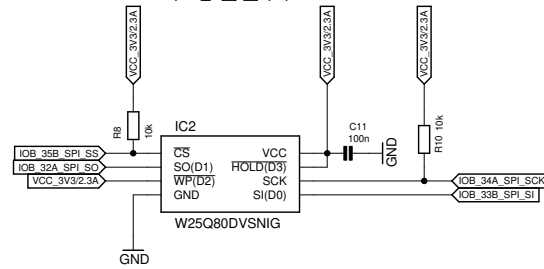
USB



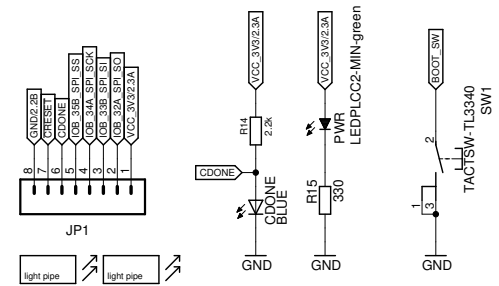
12 MHz XO



Flash



misc

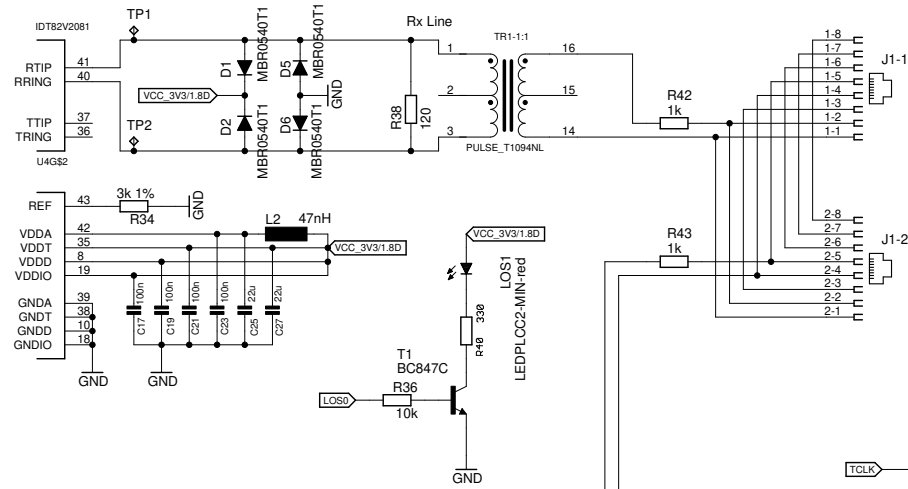
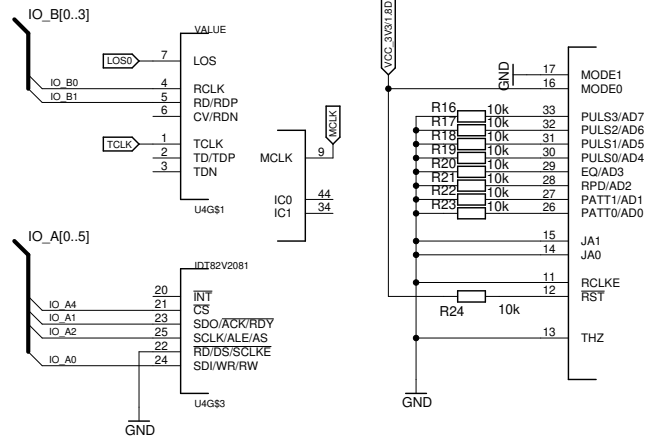


FPGA

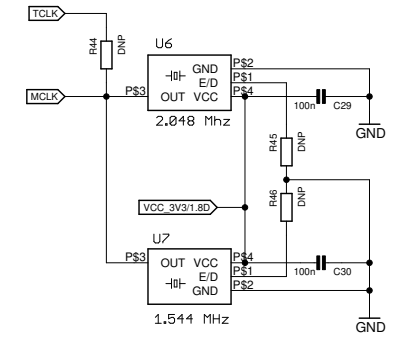
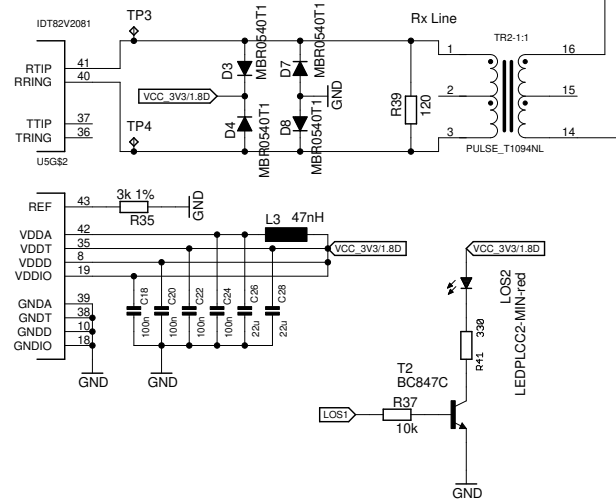
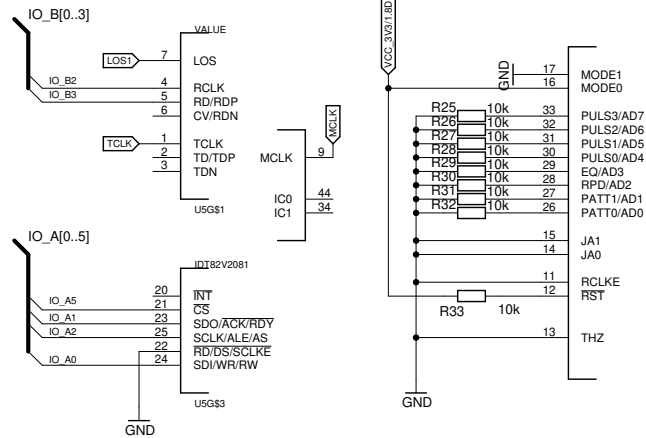
CC-BY-SA 4.0
e1-tracer v1
30.08.20 17:35
Sheet: 1/2

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LIU 0



LIU 1



- Vio - LIU power (3v3)
- GND - LIU ground
- A0 - LIU MOSI
- A1 - LIU MISO
- A2 - LIU CLK
- A3 - Debug uart TX (1 Mbaud)
- A4 - LIU CSn[0]
- A5 - LIU CSn[1]
- B0 - LIU RCLK0
- B1 - LIU RD0
- B2 - LIU RCLK1
- B3 - LIU RD1

2x LIU	CC-BY-SA 4.0
	e1-tracer v1
	30.08.20 17:35
	Sheet: 2/2